

# SERVICE MANUAL

## 3561A DYNAMIC SIGNAL ANALYZER

### VOLUME II





## SERVICE MANUAL

# MODEL 3561A DYNAMIC SIGNAL ANALYZER

Serial Prefix: 2338A

### **IMPORTANT NOTICE**

*This manual applies to instruments with the above serial number and greater. As changes are made in the instrument to improve performance and reliability, the appropriate pages will be revised to include this information.*

### **WARNING**

*To prevent potential fire or shock hazard, do not expose instrument to rain or moisture.*

Manual Part No. 03561-90010

Microfiche Part No. 03561-90060

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### **CERTIFICATION**

*Hewlett-Packard Company certifies that this product met its published specifications at the time of shipment from the factory. Hewlett-Packard further certifies that its calibration measurements are traceable to the United States National Bureau of Standards, to the extent allowed by the Bureau's calibration facility, and to the calibration facilities of other International Standards Organization members.*

### **WARRANTY**

This Hewlett-Packard product is warranted against defects in material and workmanship for a period of one year from date of shipment [except that in the case of certain components listed in Section I of this manual, the warranty shall be for the specified period]. During the warranty period, Hewlett-Packard Company will, at its option, either repair or replace products which prove to be defective.

For warranty service or repair, this product must be returned to a service facility designated by -hp-. Buyer shall prepay shipping charges to -hp- and -hp- shall pay shipping charges to return the product to Buyer. However, Buyer shall pay all shipping charges, duties, and taxes for products returned to -hp- from another country.

HP software and firmware products which are designated by HP for use with a hardware product, when properly installed on that hardware product, are warranted not to fail to execute their programming instructions due to defects in materials and workmanship. If HP receives notice of such defects during the warranty period, HP shall repair or replace software media and firmware which do not execute their programming instructions due to such defects. HP does not warrant that the operation of the software, firmware or hardware shall be uninterrupted or error free.

### **LIMITATION OF WARRANTY**

The foregoing warranty shall not apply to defects resulting from improper or inadequate maintenance by Buyer, Buyer-supplied software or interfacing, unauthorized modification or misuse, operation outside of the environmental specifications for the product, or improper site preparation or maintenance.

**NO OTHER WARRANTY IS EXPRESSED OR IMPLIED. HEWLETT-PACKARD SPECIFICALLY DISCLAIMS THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.**

### **EXCLUSIVE REMEDIES**

**THE REMEDIES PROVIDED HEREIN ARE BUYER'S SOLE AND EXCLUSIVE REMEDIES. HEWLETT-PACKARD SHALL NOT BE LIABLE FOR ANY DIRECT, INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES, WHETHER BASED ON CONTRACT, TORT, OR ANY OTHER LEGAL THEORY.**

### **ASSISTANCE**

*Product maintenance agreements and other customer assistance agreements are available for Hewlett-Packard products.*

*For any assistance, contact your nearest Hewlett-Packard Sales and Service Office. Addresses are provided at the back of this manual.*



## SAFETY SUMMARY

**The following general safety precautions must be observed during all phases of operation, service, and repair of this instrument. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of the instrument. Hewlett-Packard Company assumes no liability for the customer's failure to comply with these requirements. This is a Safety Class 1 instrument.**

### **GROUND THE INSTRUMENT**

To minimize shock hazard, the instrument chassis and cabinet must be connected to an electrical ground. The instrument is equipped with a three-conductor ac power cable. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet. The power jack and mating plug of the power cable meet International Electrotechnical Commission (IEC) safety standards.

### **DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE**

Do not operate the instrument in the presence of flammable gases or fumes. Operation of any electrical instrument in such an environment constitutes a definite safety hazard.

### **KEEP AWAY FROM LIVE CIRCUITS**

Operating personnel must not remove instrument covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

### **DO NOT SERVICE OR ADJUST ALONE**

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

### **USE CAUTION WHEN EXPOSING OR HANDLING THE CRT**

Breakage of the Cathode-ray Tube (CRT) causes a high-velocity scattering of glass fragments (implosion). To prevent CRT implosion, avoid rough handling or jarring of the instrument. Handling of the CRT shall be done only by qualified maintenance personnel using approved safety mask and gloves.

### **DO NOT SUBSTITUTE PARTS OR MODIFY INSTRUMENT**

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification to the instrument. Return the instrument to a Hewlett-Packard Sales and Service Office for service and repair to ensure that safety features are maintained.

### **DANGEROUS PROCEDURE WARNINGS**

Warnings, such as the example below, precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

### **WARNING**

**Dangerous voltages, capable of causing death, are present in this instrument. Use extreme caution when handling, testing, and adjusting.**



## SAFETY SYMBOLS

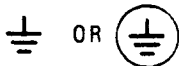
### General Definitions of Safety Symbols Used On Equipment or In Manuals.



Instruction manual symbol: the product will be marked with this symbol when it is necessary for the user to refer to the instruction manual in order to protect against damage to the instrument.



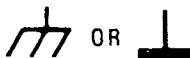
Indicates dangerous voltage (terminals fed from the interior by voltage exceeding 1000 volts must be so marked).



Protective conductor terminal. For protection against electrical shock in case of a fault. Used with field wiring terminals to indicate the terminal which must be connected to ground before operating equipment.



Low-noise or noiseless, clean ground (earth) terminal. Used for a signal common, as well as providing protection against electrical shock in case of a fault. A terminal marked with this symbol must be connected to ground in the manner described in the installation (operating) manual, and before operating the equipment.



Frame or chassis terminal. A connection to the frame (chassis) of the equipment which normally includes all exposed metal structures.



Alternating current (power line).



Direct current (power line).



Alternating or direct current (power line).

**WARNING**

The WARNING sign denotes a hazard. It calls attention to a procedure, practice, condition or the like, which, if not correctly performed or adhered to, could result in injury or death to personnel.

**CAUTION**

The CAUTION sign denotes a hazard. It calls attention to an operating procedure, practice, condition or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product.

**NOTE :**

The NOTE sign denotes important information. It calls attention to procedure, practice, condition or the like, which is essential to highlight.

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**SECTION VII**  
**SCHEMATICS/SERVICE**

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## SECTION VII SERVICE

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### 7-1 INTRODUCTION

The information contained in this section is used for troubleshooting a circuit board to the component level. The following information is given for each board: circuit description, troubleshooting procedures, component locator, and schematic diagram. A complete list of schematic diagrams is given in Table 7-1.

The equipment needed to perform the troubleshooting procedures is listed in Table 1-5. If the recommended equipment is not available, a substitute may be used which meets or exceeds the critical specifications listed in the table.

#### NOTE

*After completing a test or repair, check that all jumpers have been returned to the NORMAL or RUN position and that all cables have been re-connected.*

#### CAUTION

*Do not remove or replace any circuit boards when the LINE power switch is ON.*

#### CAUTION

*To protect the -hp-3561A circuits from static discharge, remove or replace circuit boards only at static protected work stations.*

**Table 7-1 Schematic Diagrams**

Schematic/ Assembly Number	Number of Schematics	Board Description
A10	2	Input Amplifier
A15	2	Digitizer
A20	4	Digital Filter
A30	2	FFT/RAM
A40	4	Processor/ROM
A50	3	Local Oscillator/Noise Source
A60	3	Digital Display Driver
A65	1	CMOS/Bubble Memory
A66	1	CMOS Memory
A70, A71, A72	2	Power Supply
A80, A81	1	Keyboard
A82	1	Rear Panel
A90	1	Analog Display Driver

## 7-2 SAFETY CONSIDERATIONS

### WARNING

*Maintenance described herein is performed with power supplied to the instrument and with the protective covers removed. Such maintenance should be performed only by service-trained personnel who are aware of the hazards involved.*

*Any interruption of the protective grounding conductor inside or outside the instrument, or disconnection of the protective earth terminal, is likely to make the instrument hazardous.*

### WARNING

*±170 Volts are present on the A70 and A71 Assemblies. ±170 Volts are present on the heat sinks on the A70 Assembly. This voltage is exposed whenever the protective power supply cover is removed. Be extremely careful when working in proximity to this area. The high voltage can cause serious personal injury if contacted.*

### WARNING

*Capacitors in the power supply will remain charged to ±170 Volts dc for at least three(3) minutes after power is removed from the instrument. Do not remove the power supply assemblies (A70, A71, A72) or disconnect cables W70 or W71 for at least three(3) minutes after power is removed from the -hp-3561A.*

### WARNING

*Only fuses with the required current rating and of the specified type should be used for replacement. The use of repaired fuses or short circuiting the fuse holder is not permitted. Whenever it is likely that the protection offered by the fuse has been impaired, the instrument must be made inoperative, and secured against any unintended operation.*








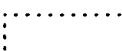


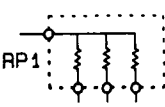

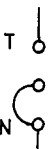
### WARNING

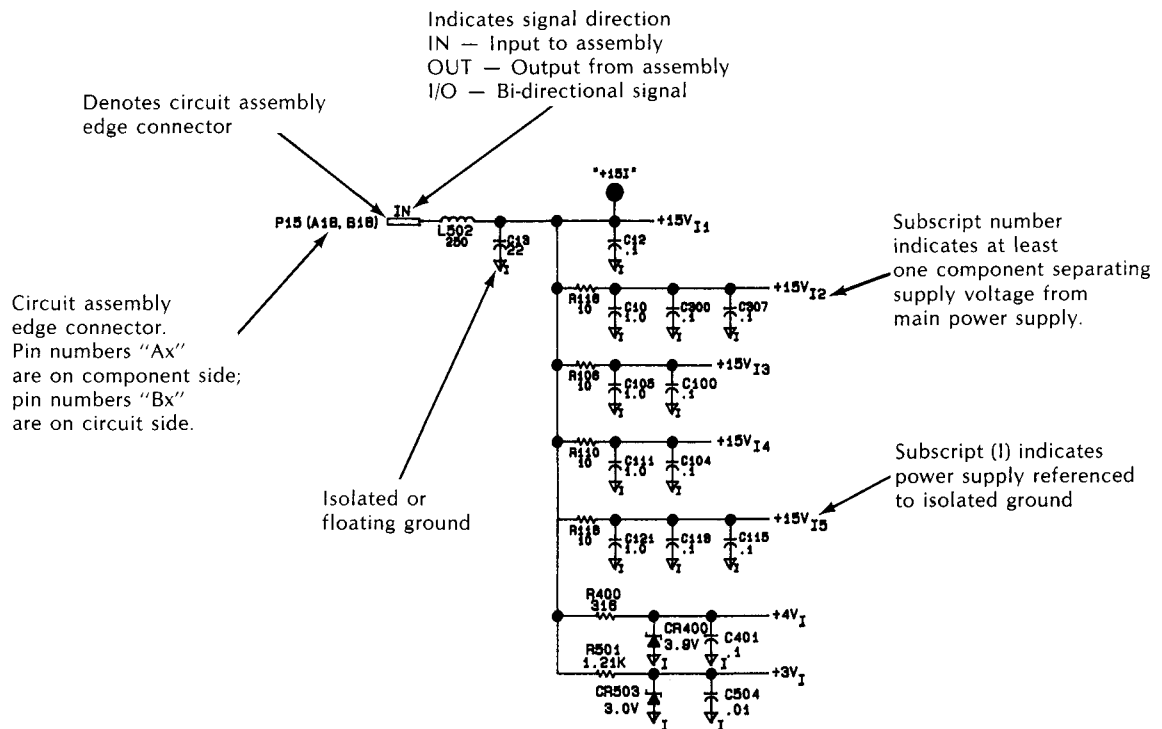
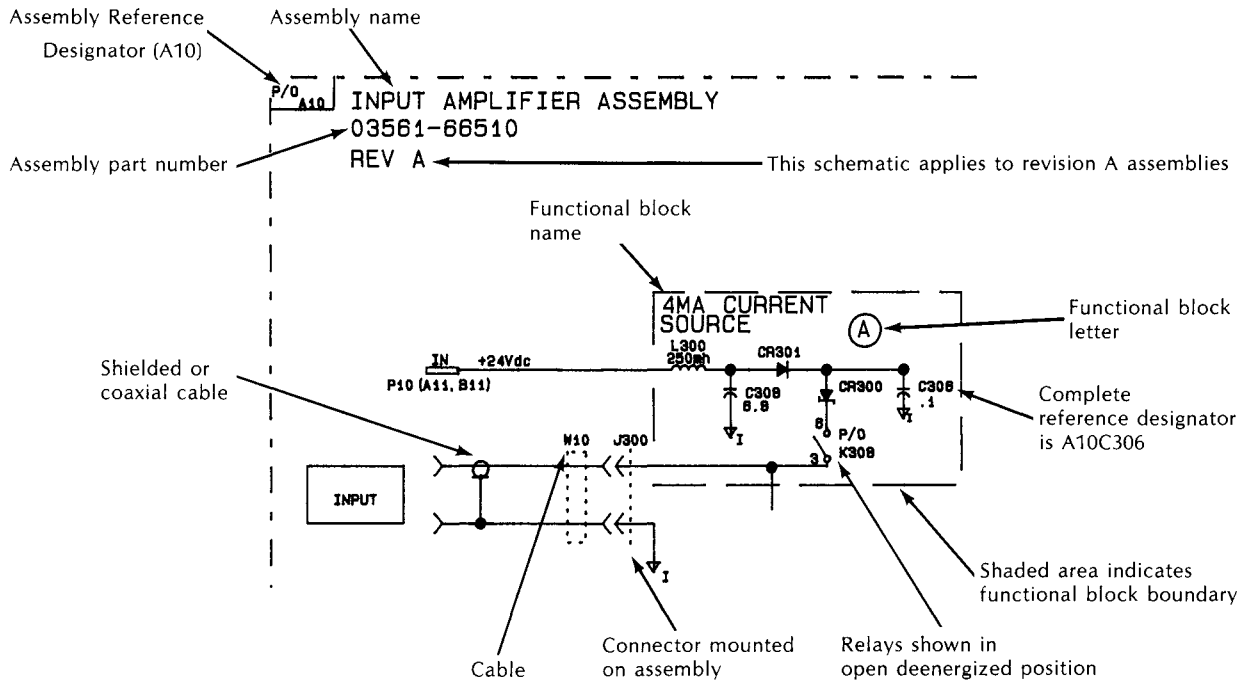
*The protective power supply covers are removed exposing ±170 Volts while troubleshooting the A66 CMOS Memory Assembly or the A65 CMOS/Bubble Memory Assembly. Be extremely careful when working in this area, the high voltage could cause serious personal injury if contacted.*

**WARNING**

*+8000 Volts are present in the CRT AT ALL TIMES, EVEN WHEN POWER IS REMOVED FROM THE INSTRUMENT! Be extremely careful when working in proximity to this area. The high voltage can cause serious personal injury if contacted.*

**7-3 SCHEMATIC NOTES**

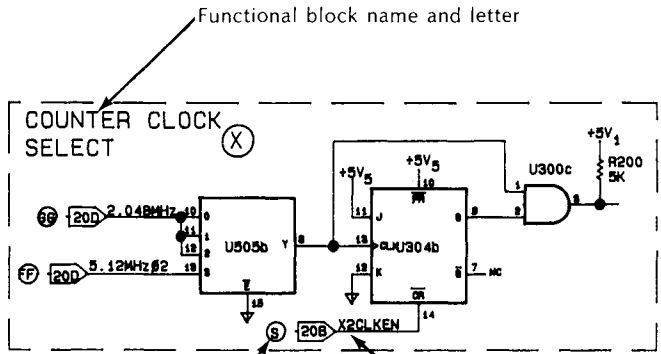
<p>1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. PREFIX WITH ASSEMBLY DESIGNATION FOR COMPLETE DESIGNATION.</p> <p>2. COMPONENT VALUES ARE SHOWN AS FOLLOWS UNLESS OTHERWISE NOTED. RESISTANCE IN OHMS CAPACITANCE IN MICROFARADS INDUCTANCE IN MILLIHENRIES</p> <p>3.  DENOTES EARTH GROUND USED FOR TERMINALS WITH NO LESS THAN A NO. 18 GAUGE WIRE CONNECTED BETWEEN TERMINAL AND EARTH GROUND TERMINAL OF AC POWER RECEPTACLE</p> <p>4.  DENOTES FRAME GROUND USED FOR TERMINALS WHICH ARE PERMANENTLY CONNECTED WITHIN APPROXIMATELY 0.1 OHM OF EARTH GROUND.</p> <p>5.  DENOTES GROUND ON PRINTED CIRCUIT ASSEMBLY (ELECTRICALLY CONNECTED TO FRAME GROUND.)</p> <p>6.  DENOTES ISOLATED (I) OR SIGNAL(S) CIRCUIT GROUND.</p> <p>7.  DENOTES ASSEMBLY</p> <p>8.  DENOTES MAIN SIGNAL PATH</p> <p>9.  DENOTES FRONT PANEL MARKING</p>	<p>10.  DENOTES REAR PANEL MARKING.</p> <p>11.  DENOTES SCREWDRIVER ADJUST</p> <p>12. * AVERAGE VALUE SHOWN. OPTIMUM VALUE SELECTED AT FACTORY. THE VALUE OF THESE COMPONENTS MAY VARY FROM ONE INSTRUMENT TO ANOTHER.</p> <p>13.  DENOTES RF SHIELD</p> <p>14. ALL RELAYS ARE SHOWN DEENERGIZED. ALL ANALOG SWITCH IC'S ARE SHOWN NOT ACTIVE.</p> <p>15.  DENOTES RESISTOR PACK</p> <p>16. ALL WAVEFORMS SHOWN ARE MEASURED WITH A 10:1 OSCILLOSCOPE PROBE UNLESS OTHERWISE NOTED. ALL DC VOLTAGES ARE MEASURED WITH A 1:1 PROBE AND A DVM.</p> <p>17.  MAY BE LOADED WITH A ZERO OHM RESISTOR OR A JUMPER WIRE.</p> <p>18.  MOVEABLE JUMPER. N INDICATES NORMAL OR RUN POSITION; T INDICATES TEST POSITION.</p>
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**Schematic A20c**

P/O A20 DIGITAL FILTER ASSEMBLY  
03561-66520  
REV A



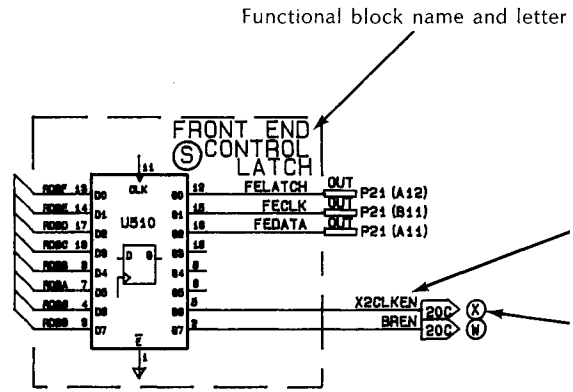
Functional block name and letter

Indicates signal source.  
This signal comes from functional block S on Schematic A20b.  
Direction of arrow indicates signal direction.

Signal name

**Schematic A20b**

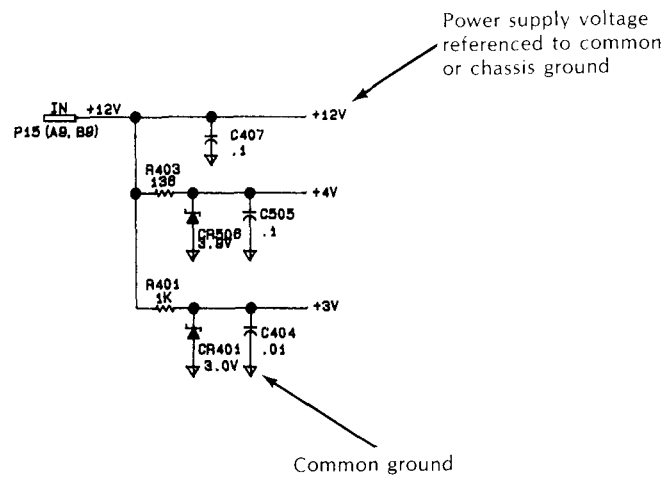
P/O A20 DIGITAL FILTER ASSEMBLY  
03561-66520  
REV A



Functional block name and letter

Signal name

Indicates signal destination.  
This signal goes to Functional block X on Schematic A20c.  
Direction of arrow indicates signal direction.



## **7-4 A10 INPUT AMPLIFIER ASSEMBLY**

### **7-5 Input Amplifier Circuit Description**

#### **GENERAL**

The main function of the Input Amplifier Assembly is to implement the RANGE function. This function allows the -hp-3561A to measure signals of different amplitudes. The range setting specifies the maximum input amplitude which will not overload the -hp-3561A. Other circuitry on the A10 Assembly includes the Auto-Zero DAC, Trigger Level DAC, and A-Weight Filter.

#### **[A] 4 mA CURRENT SOURCE, FRONT PANEL GROUND SWITCH**

When signal ICP ON/OFF is TTL high, relay K308 closes, and a 4 milliamp current is delivered to the center conductor of the BNC input connector.

The front panel ground switch determines the ground reference for the the input connector. When the ground switch is in the FLOAT position, signal FEISO is pulled low to tell the processor the position of the ground switch for HP-IB access.

#### **[B] CAL SIGNAL GENERATOR, [O] CAL SIGNAL CONTROL**

These circuits produce a signal with a precise amplitude of 195 mVrms (-14.2 dBV) which is used to calibrate the amplitude accuracy of the -hp-3561A. The cal signal frequency, which is set on the A20 Assembly, is 4 kHz when the cal signal is selected by pressing the INPUT key and selecting CAL SIG ON. To isolate the front panel input connector when the cal signal is enabled, BNC1 goes low to open K305 and K307 and BNC2 goes high to close K306. For more information, see the "Self Calibration" paragraph in Section 6 of this manual.

#### **[C] ATTENUATOR #1,[F] ATTENUATOR #2, [H] ATTENUATOR #3,[J] ATTENUATOR #4**

These attenuators are programmable through the front end control register to the attenuation values specified on the schematic. The equivalent attenuation in linear terms is also given on the schematic. The attenuators are used to scale the input signal to a nominal level for the A/D converter. Table 7-2 lists all of the attenuator setting as a function of the instrument RANGE setting.

#### **[K] A-WEIGHT FILTER**

The A-Weight Filter is enabled by the AWHT ON/OFF signal from the front end control register. The A-Weight Filter implements ANSI Standard S1.4-1971. A table of filter gain verses frequency is given in Table 7-3.

**Table 7-2 Attenuator Settings vs. Range Settings**

<b>RANGE (DBV)</b>	<b>ATTENUATOR#1 (dBV)</b>	<b>ATTENUATOR#2 (dBV)</b>	<b>ATTENUATOR#3 (dBV)</b>	<b>ATTENUATOR#4 (dBV)</b>
+27	40	12	12	14
+26	40	13	10	14
+25	40	12	10	14
+24	40	13	8	14
+23	40	12	8	14
+22	40	13	6	14
+21	40	12	6	14
+20	40	13	4	14
+19	40	12	4	14
+18	40	13	2	14
+17	40	12	2	14
+16	40	1	12	14
+15	40	0	12	14
+14	40	1	10	14
+13	40	0	10	14
+12	40	1	8	14
+11	40	0	8	14
+10	40	1	6	14
+9	40	0	6	14
+8	40	1	4	14
+7	20	12	12	14
+6	20	13	10	14
+5	20	12	10	14
+4	20	13	8	14
+3	20	12	8	14
+2	20	13	6	14
+1	20	12	6	14
0	20	13	4	14
-1	20	12	4	14
-2	20	13	2	14
-3	20	12	2	14
-4	20	1	12	14
-5	20	0	12	14
-6	20	1	10	14
-7	20	0	10	14
-8	20	1	8	14
-9	20	0	8	14
-10	20	1	6	14
-11	20	0	6	14
-12	20	1	4	14
-13	0	12	12	14
-14	0	13	10	14
-15	0	12	10	14
-16	0	13	8	14
-17	0	12	8	14
-18	0	13	6	14
-19	0	12	6	14
-20	0	13	4	14
-21	0	12	4	14
-22	0	13	2	14
-23	0	12	2	14
-24	0	1	12	14
-25	0	0	12	14
-26	0	1	10	14
-27	0	0	10	14

**Table 7-2 Attenuator Settings vs. Range Settings (Cont'd)**

<b>RANGE (DBV)</b>	<b>ATTENUATOR#1 (dBV)</b>	<b>ATTENUATOR#2 (dBV)</b>	<b>ATTENUATOR#3 (dBV)</b>	<b>ATTENUATOR#4 (dBV)</b>
-28	0	1	8	14
-29	0	0	8	14
-30	0	1	6	14
-31	0	0	6	14
-32	0	1	4	14
-33	0	0	4	14
-34	0	1	2	14
-35	0	0	2	14
-36	0	1	0	14
-37	0	0	0	14
-38	0	1	0	12
-39	0	0	0	12
-40	0	1	0	10
-41	0	0	0	10
-42	0	1	0	8
-43	0	0	0	8
-44	0	1	0	6
-45	0	0	0	6
-46	0	1	0	4
-47	0	0	0	4
-48	0	1	0	2
-49	0	0	0	2
-50	0	1	0	0
-51	0	0	0	0

**[L] AUTO-ZERO DAC**

The auto-zero DAC is programmed through the front end control register to zero the dc offset in the input circuitry. An auto-zero is performed whenever a calibration is performed or the instrument range is changed. This function can be disabled by moving jumper A10W100 to the test position.

**[N] DIGITAL CONTROL INPUT AND ISOLATION**

The FEDATA, FECLOCK and FELATCH signals work together to input, clock, and latch digital information from the processor into the front end control register. These three signals are transformer coupled to maintain isolation between the chassis ground and the isolated ground.

**[P] FRONT END CONTROL REGISTER**

The front end control register is a serial in parallel out register which latches and stores A10 Assembly programming data. Data stored in the front end control register is only updated when an instrument front panel control is changed which requires a change in the setup of the A10 Assembly or the A15 Assembly.

**Table 7-3 A-Weight Filter Characteristics**

Frequency (Hz)	Amplitude Gain (dB)	Tolerance (dB)
10.0	-70.4	± 4.0
12.5	-63.4	± 3.5
16.0	-56.7	± 3.0
20.0	-50.5	± 2.5
25.0	-44.7	± 2.0
31.5	-39.4	± 1.5
40.0	-34.6	± 1.5
50.0	-30.2	± 1.0
63.0	-26.2	± 1.0
80.0	-22.5	± 1.0
100	-19.1	± 1.0
125	-16.1	± 1.0
160	-13.4	± 1.0
200	-10.9	± 1.0
250	-8.6	± 1.0
315	-6.6	± 1.0
400	-4.8	± 1.0
500	-3.2	± 1.0
630	-1.9	± 1.0
800	-0.8	± 1.0
1000	0	± 1.0
1250	0.6	± 1.0
1600	1.0	± 1.0
2000	1.2	± 1.0
2500	1.3	± 1.0
3150	1.2	± 1.0
4000	1.0	± 1.0
5000	-0.5	+1.5,-2
6300	-0.8	+1.5,-2
8000	-1.1	+1.5,-3
10000	-2.5	+2,-4
12500	-4.3	+3,-6
16000	-6.6	+3,-∞
20000	-9.3	+3,-∞

**[Q] TRIGGER LEVEL DAC**

The Trigger Level DAC is used to set up the voltage level at which the -hp-3561A will trigger on the input signal. The trigger level is established by the DEFINE % OF RNG soft key. A trigger level of 100 % of range corresponds to a DAC output of 1.29 Vdc regardless of the range selected. The DAC output for other percentage settings may be directly calculated by taking the percentage selected of 1.29 Vdc (eg., .645 Vdc for a 50 % setting).

**Table 7-4 A10 Assembly Signal Descriptions**

<b>Signal Name</b>	<b>Description</b>
AC/DC CPL	AC/DC CouPLing: TTL high for dc coupling of the input signal, low for ac coupling.
ATTN1 - ATTN4	ATTeNuator #1 through ATTeNuator #4: These signals program the attenuation of the four input attenuators.
BNC1	Isolates the front panel BNC connector when the CAL BNC2 signal is enabled.
COMP OUT	COMPare OUTput: This signal is used on the A15 Assembly to generate the over-range, under-range, and input trigger signals.
FE CAL	Front End CALibration: TTL signal from the A20 Assembly which sets the frequency of the CAL signal used for self calibration.
FE CALG	Front End CALibration Gated: FE CAL gated by CAL ON/OFF Signal.
FECLOCK	Front End CLOCK: Clocks the FEDATA signal into the front end control register.
FEDATA	Front End DATA: Serial data which programs all circuits on the A10 Assembly when latched into the front end control register.
FEDATAIC	Front End DATA Isolated Continue: A continuation of the FEDATA signal. This signal contains programming information for the A15 Assembly.
FELATCH	Front End LATCH: Latches the FEDATA signal into the front end control register.
TRIG0-7	TRIGger bus (0-7): Programs the trigger level D/A converter.
0DAC0-7	0 Digital to Analog Converter bus (0-7): Programs the auto zero D/A converter.

### 7-6 Troubleshooting the Input Amplifier



*Before removing the A10 Assembly, remove the bottom cover and disconnect the input cable (W10).*

#### GENERAL

The primary method for troubleshooting this assembly is to input a sine wave to the -hp-3561A and check the signal at each amplifier stage. Table 7-5 lists the signal amplitudes at the AMP1, AMP2, and AMP3 test points and at the A10 output (J200) for an input sine wave with an amplitude equal to the -hp-3561A range setting.

All signal amplitudes listed have a tolerance of  $\pm 5\%$  ( $\pm .4$  dB)

**[C] ATTENUATOR #1,[E] AMPLIFIER #1,[F] ATTENUATOR #2,[G] AMPLIFIER #2,  
[H] ATTENUATOR #3,[I] AMPLIFIER #3,[J] ATTENUATOR #4,[M] AMPLIFIER #4**

To check these circuits, place the A10 Assembly on an extender board and use a BNC to SMB adapter cable to input a 1 kHz, 1 Vrms (1.414 Vpeak) sine wave into A10J10. Set the -hp-3561A controls as follows:

PRESET  
RANGE ..... DEFINE RANGE ..... 0 dBV

Verify the signal amplitudes listed in the 0 dBV range column of Table 7-5. This test can be repeated at the other range settings listed.

**Table 7-5 Signal Amplitudes vs. Range Setting**

-hp-3561A RANGE SETTING	dBV Vrms Vpeak	+9 2.818 3.985	0 1.00 1.414	-5 .5623 .7952	-36 .0158 .0223	-51 .0028 .0039
TP AMP1	dBV Vrms Vpeak	-21.46 .085 .120	-10.46 .300 .424	-15.46 .168 .238	-26.46 .047 .066	-41.56 .0085 .012
TP AMP2	dBV Vrms Vpeak	-11.92 .254 .359	-13.92 .201 .284	-5.92 .506 .716	-17.92 .127 .180	-31.92 .025 .035
TP AMP3	dBV Vrms Vpeak	-8.37 .381 .539	-8.37 .381 .539	-8.37 .381 .539	-8.37 .381 .539	-22.37 .076 .107
OUTPUT	dBV Vrms Vpeak	-12.83 .228 .323	-12.83 .228 .323	-12.83 .228 .323	-12.83 .228 .323	-12.83 .228 .323

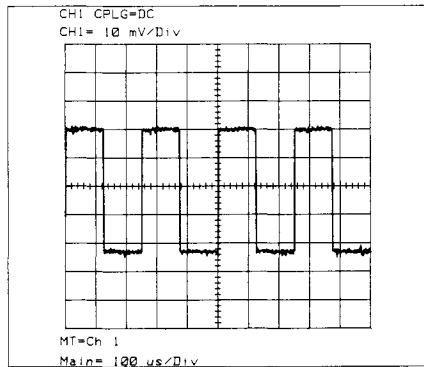


**[B] CAL SIGNAL GENERATOR, [O] CAL SIGNAL CONTROL**

To check these circuits, set the -hp-3561A controls as shown below, and use a digital voltmeter to check for .216 Vac at the CAL test point. Verify the CAL signal as shown in Figure 7-1.

PRESET  
 INPUT..... AUTO CAL OFF  
 CAL SIG ON

**Figure 7-1 CAL Signal Waveform**



Probe: 10:1  
 Ch1: Connection- A10 TP CAL  
 Coupling- dc  
 Ground- Center Graticule  
 Trigger: Internal- Ch1  
 Slope- Positive  
 Bandwidth Limit: OFF

**Troubleshooting for Distortion**

To troubleshoot for distortion failures, a low distortion oscillator, which meets the required characteristics listed in Table 1-5, is used to input a sine wave to each of the test points AMP1, AMP2, AMP3, and to A15J1. The -hp-3561A display can then be monitored for distortion introduced by each amplifier stage.

1. Set the -hp-3561A controls as follows:

PRESET  
 INPUT..... AUTO CAL OFF

2. Disconnect cable W15 from connector A15J1 and move test jumper A10W100 to the TEST position.
3. Using a BNC to SMB adapter cable and the low distortion oscillator, input a 1 kHz, .228 Vrms( $\pm 5\%$ ) sine wave into A15J1. If all harmonics are greater than 80 dB below the 1 kHz fundamental, the -hp-3561A main measurement path through the A15, A20, and A30 Assemblies is operating correctly. This main measurement path can now be used to test the A10 Assembly. If a full scale 1 kHz sine wave does not appear on the display, or the harmonic signals are less than 80 dB below the fundamental, troubleshoot the A15, A20, and A30 Assemblies before troubleshooting distortion on the A10 Assembly.
4. Reconnect cable W15 to connector A15J1.

- Set the -hp-3561A controls as follows:

RANGE ..... DEFINE RANGE .....-51 dBV

- Connect a 50Ω termination to A10J300 through a BNC to SMB adapter cable.
- Using a clip lead or a shielded connector, input a 1 kHz, 76 mVrms (±5%) sine wave to the AMP3 test point. If all harmonics are greater than 80 dB below the 1 kHz fundamental, the circuits between the AMP3 test point and A10J200 are operating correctly.

- Set the -hp-3561A controls as follows:

RANGE ..... DEFINE RANGE .....-36 dBV

- Using a clip lead or a shielded connector, input a 1 kHz, 127 mVrms (±5%) sine wave to the AMP2 test point. If all harmonics are greater than 80 dB below the carrier, the circuits between the AMP2 test point and A10J200 are operating correctly.

- Set the -hp-3561A controls as follows:

RANGE ..... DEFINE RANGE .....-5 dBV

- Using a clip lead or a shielded connector, input a 1 kHz, 169 mVrms (±5%) sine wave to the AMP1 test point. If all harmonics are greater than 80 dB below the 1 kHz fundamental, the circuits between the AMP1 test point and A10J200 are operating correctly.

- Move test jumper A10W100 back to NORM position, and reconnect cable W15 to connector A15J1.

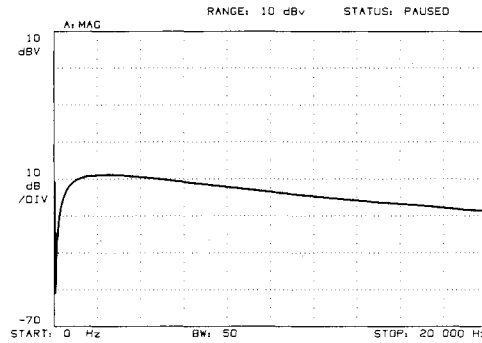
**[K] A-WEIGHT FILTER**

To check the A-Weight Filter for proper operation, connect the -hp-3561A noise source output to the -hp-3561A input connector and set the -hp-3561A controls as follows:

PRESET  
 WINDOW ..... UNIFORM  
 SOURCE ..... PERIODIC NOISE  
 DEFINE ATTEN ..... 0 dB  
 FREQUENCY ..... DEFINE SPAN ..... 20 kHz  
 INPUT ..... A WT FLT ON  
 FORMAT ..... SINGLE

Check the frequency response by varying the -hp-3561A frequency span. To check for distortion or noise, input a sine wave rather than the noise signal to the -hp-3561A. Table 7-3 lists the A-Weight Filter gain for various frequencies.

**Figure 7-2 A-Weight Filter Response**



**[A] 4 mA CURRENT SOURCE**

To check the 4 mA ICP Current Source for proper operation, terminate the -hp-3561A input port with a 50Ω load and set the -hp-3561A controls as follows:

```
PRESET
INPUT..... ICP CURR ON
```

Use a digital voltmeter to check the voltage across the 50Ω load for approximately .2 Vdc. If the voltage is incorrect, check the +24 V power supply and the current source circuitry.

**[Q] Trigger Level DAC**

The output of the trigger level DAC may be monitored at the TRG test point. To troubleshoot the DAC, set the -hp-3561A controls as follows:

```
RESET
RANGE..... AUTO RNG OFF
TRIGger SElect... INPUT TRIGGER
                SETUP SELECT ... DEFINE % OF RNG .....100 %
```

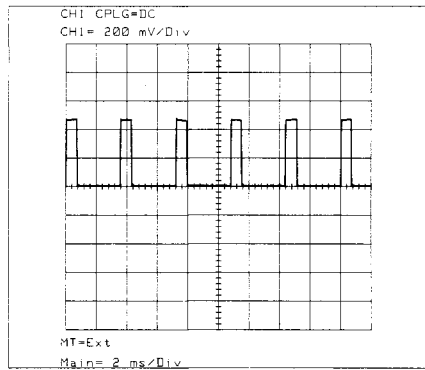
The DAC output should be 1.29 ± .13 Vdc. Vary the % of range selected and check the corresponding DAC output voltage (eg: a trigger level of 50 % of range will result in a .645 Vdc output).

**[N] Digital Control Input and Isolation, [P] Front End Control Register**

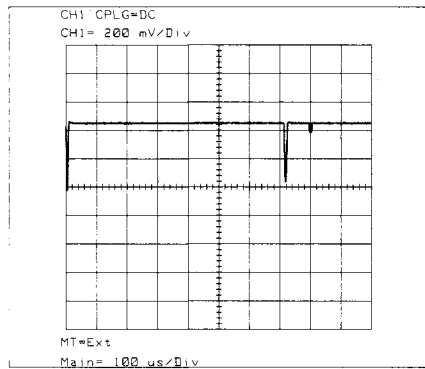
To check the these circuits, select self test 110 as follows, and check the waveforms shown in Figure 7-3.

```
PRESET
MODE ..... TEST SELECT..... DEFINE TEST NUM.....110 ENTER
                START CONT TEST
```

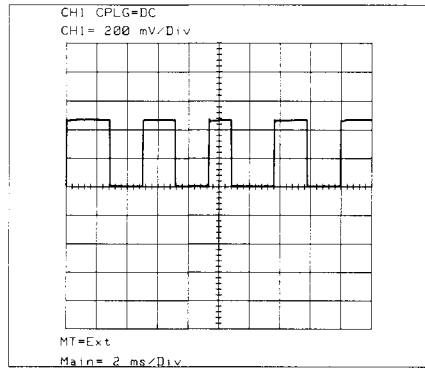
**Figure 7-3 Front End Control Register Waveforms**



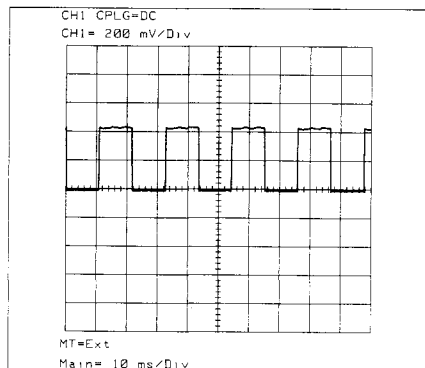
Probe: 10:1  
 Ch1: Connection- A10 U400(10) "FELATCHI"  
 Coupling- dc  
 Ground- Center Graticule  
 Trigger: External- A20 J200(5)  
 Slope: Positive  
 Bandwidth Limit: OFF



Probe: 10:1  
 Ch1: Connection- A10 U402(9) "FECLKI"  
 Coupling- dc  
 Ground- Center Graticule  
 Trigger: Internal- Ch1  
 Slope: Negative  
 Bandwidth Limit: OFF



Probe: 10:1  
 Ch1: Connection- A10 U402(13) "FEDATAI"  
 Coupling- dc  
 Ground- Center Graticule  
 Trigger: External- A20 J200(5)  
 Slope: Positive  
 Bandwidth Limit: OFF



Probe: 10:1  
 Ch1: Connection-  
 This waveform is available at any of the following connection points. The waveform will be shifted in time relative to the external trigger at each different connection point.  
 U401(4,5,6,7,11,12,13,14)  
 U201(4,5,6,7,11,12,13,14)  
 U105(4,5,6,7,11,12,13,14)  
 U107(4,5,6,7,11,12,13,14)  
 Coupling- dc  
 Ground- Center Graticule  
 Trigger: External- A20 J200(5)  
 Slope: Positive  
 Bandwidth Limit: OFF

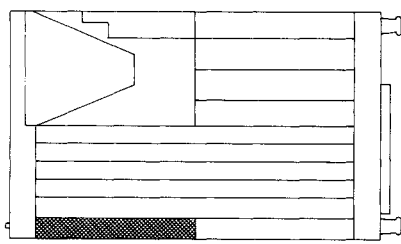
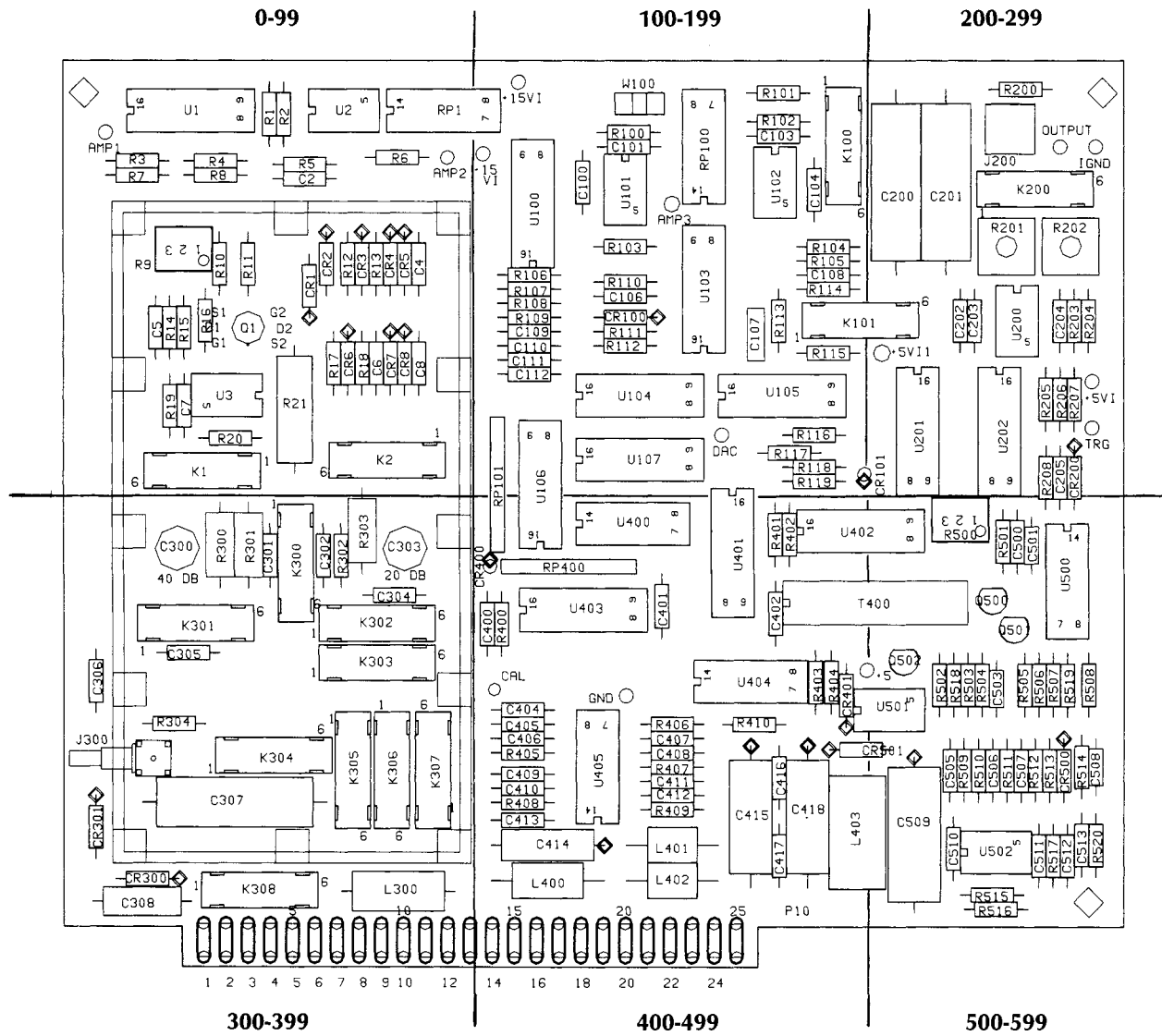
**Table 7-6 A10 Assembly Signal Connections**

**INPUTS**

<b>Signal Name</b>	<b>Functional Block</b>	<b>Connector Number</b>	<b>Origin Assembly</b>
FE CAL	N	P10(A15)	A20
FECLOCK	N	P10(A16)	A20
FEDATA	N	P10(B16)	A20
FELATCH	N	P10(B15)	A20
INPUT	A	J10	Front panel
+ 24 V	A	P10(A11)	A99

**OUTPUTS**

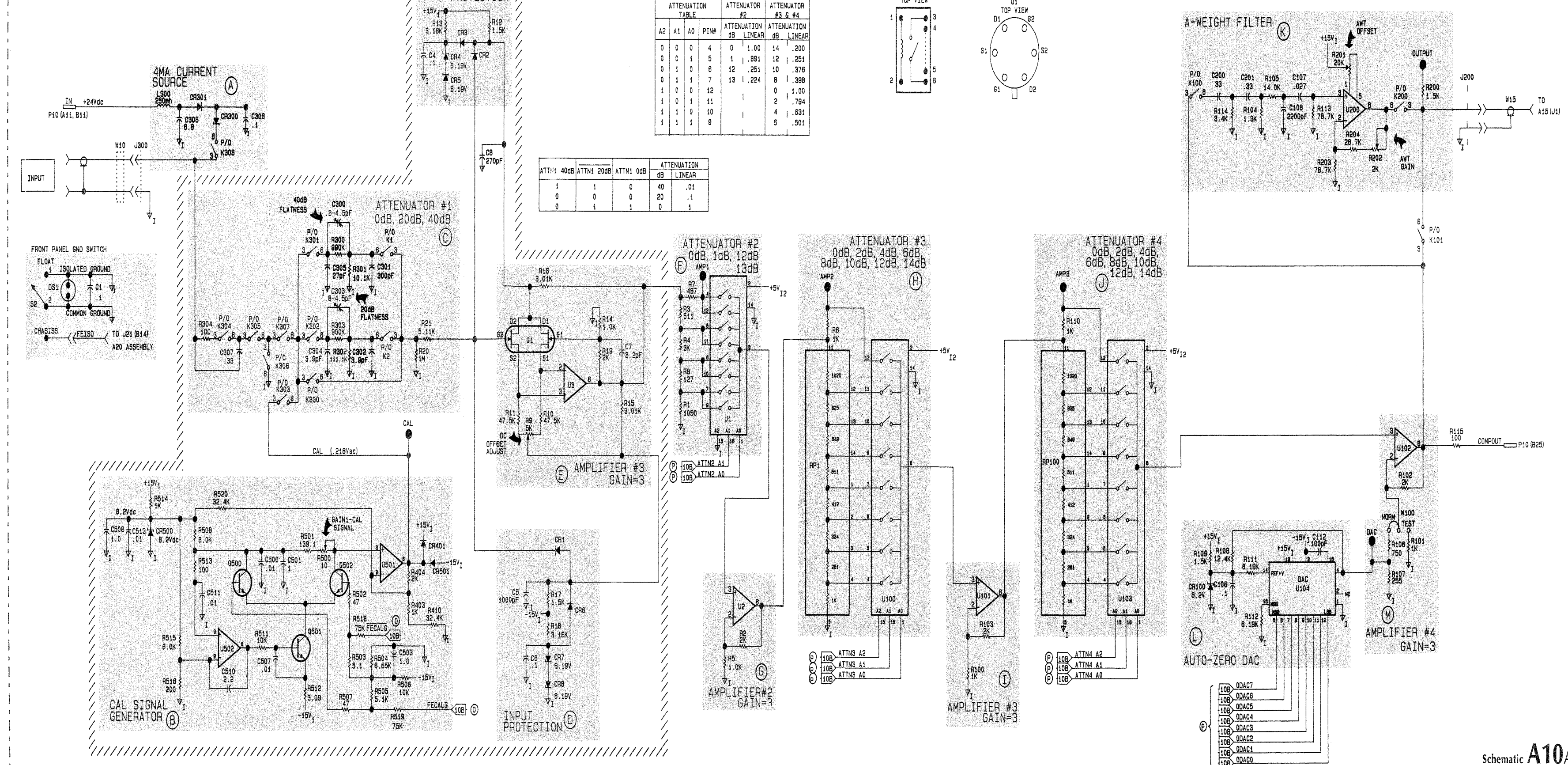
<b>Signal Name</b>	<b>Functional Block</b>	<b>Connector Number</b>	<b>Destination Assemblies</b>
COMP OUT	M	P10(B25)	A15
FECLK	P	P10(A24)	A15
FEDATA	P	P10(A25)	A15
FEISO	A	A99 J11	A20
FELATCH	P	P10(A23)	A15
SIGNAL OUT	K	J200	A15



A10 Assembly

	+15V <sub>I</sub>	+15V <sub>II</sub>	-15V <sub>I</sub>	-15V <sub>II</sub>	+5V <sub>I</sub>	GND <sub>I</sub>	+5V <sub>II</sub>	GND <sub>II</sub>	By-Pass Capacitors
U1	13		3						C110, C109
U2	7		4						
U3	7		4						C101, C100
U100	13		3						C103, C104
U101	7		4						
U102	7		4						C202
U103	13		3						
U104	13		3						
U105					16	8			
U106					9	8			
U107					16	8			
U200	7		4						C204
U201					16	8			
U202	13		3						
U400					14	7			
U401					16	8			
U402					16	8			
U403					9	8			
U403					14	7			
U500					14	7	14	7	
U501	7		4						
U502		7		4					

INPUT AMPLIFIER ASSEMBLY  
03561-66510  
REV B

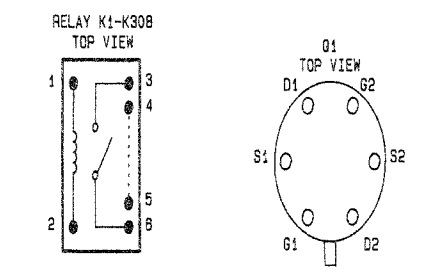


ATTENUATION TABLE

A2	A1	A0	PIN#	ATTENUATOR #2 dB LINEAR	ATTENUATOR #3 & #4 dB LINEAR
0	0	0	4	0	1.00
0	0	1	5	1	.881
0	1	0	6	12	.251
0	1	1	7	13	.224
1	0	0	12		0
1	0	1	11		2
1	1	0	10		4
1	1	1	9		5

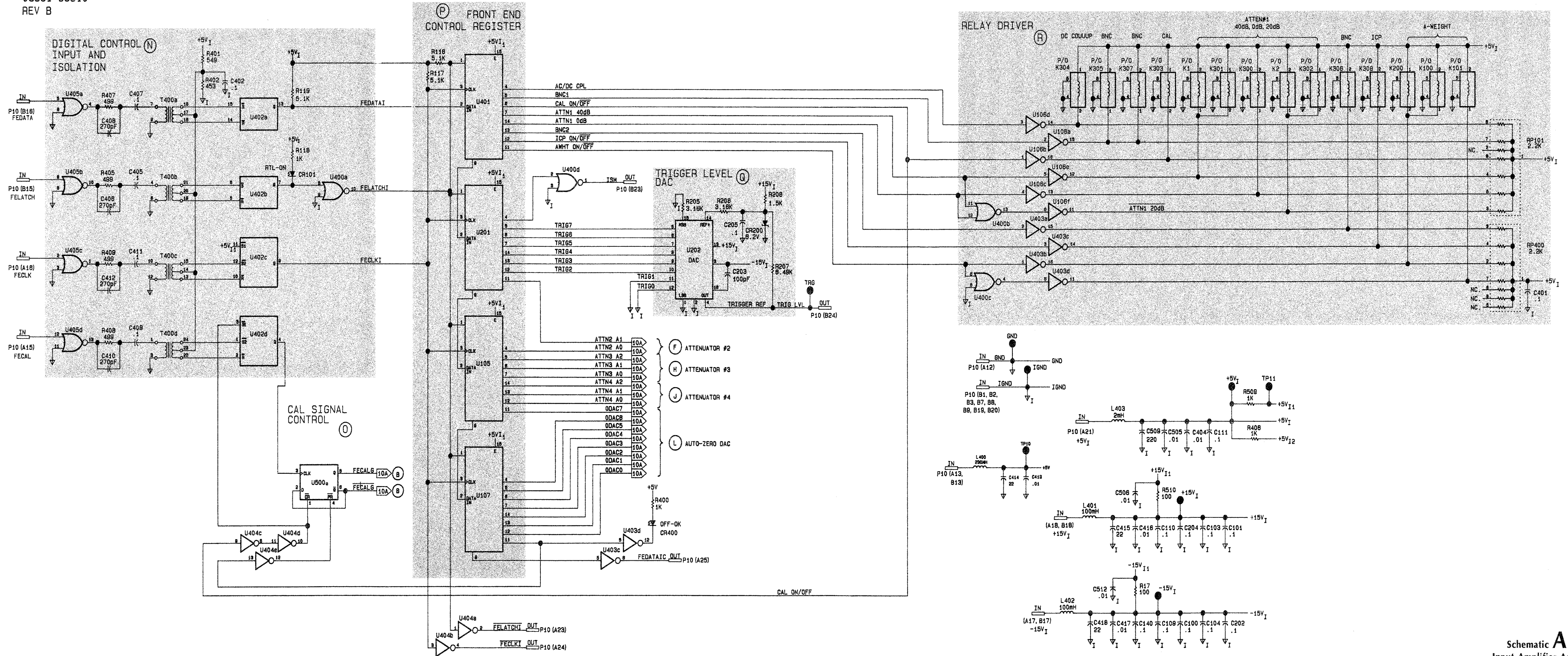
ATTENUATION

ATTN1	ATTN2	ATTN3	dB	LINEAR
1	1	0	40	.01
0	0	0	20	.1
0	0	1	0	1





**A10** INPUT AMPLIFIER ASSEMBLY  
03561-66510  
REV B



**Schematic A10B**  
Input Amplifier Assembly  
7-21/7-22



## **7-7 A15 DIGITIZER ASSEMBLY**

### **7-8 Digitizer Circuit Description**

#### **GENERAL**

The A15 Assembly uses a "two-pass residue" type A/D converter to digitize the analog input signal into a 13 bit digital output. A track and hold circuit samples the input signal and holds it long enough for the analog to digital conversion to take place. In addition the A15 Assembly contains a 100 kHz low-pass filter to attenuate higher frequency signals which may interact with the measurement. Other circuits on the assembly include the over-range and half-range comparators, the trigger level comparators, a test register, and a ground isolation interface.

Figure 7-4 gives a timing diagram of the complete analog to digital conversion process. The heart of the A15 Assembly digitizer is a single chip, 8 bit A/D converter which will be referred to as the "8 bit ADC". Each complete analog to digital conversion consists of two passes of data through the 8 bit ADC. In the first pass, the track and hold output signal is input to the 8 bit ADC. The result of the first pass conversion is an 8 bit digital approximation to the analog track and hold output. The timing and control circuit then transfers this 8 bit digital signal to the second pass input circuit. In the second pass, the result of the first pass conversion is converted back into an analog signal and subtracted from the analog track and hold output, resulting in a signal that is equal to the error between the first pass 8 bit approximation and the track and hold output. This error signal is multiplied by 32 and input to the 8 bit ADC. The second pass conversion is then scaled back down by 32 and added to the first pass conversion to obtain a final 13 bit digital result.

Between each conversion, the 8 bit ADC is reset by passing a fixed dc voltage of .34 volts through it. The dc voltage is derived from the the 6.2 volt reference and is selected by the ADC input switch.

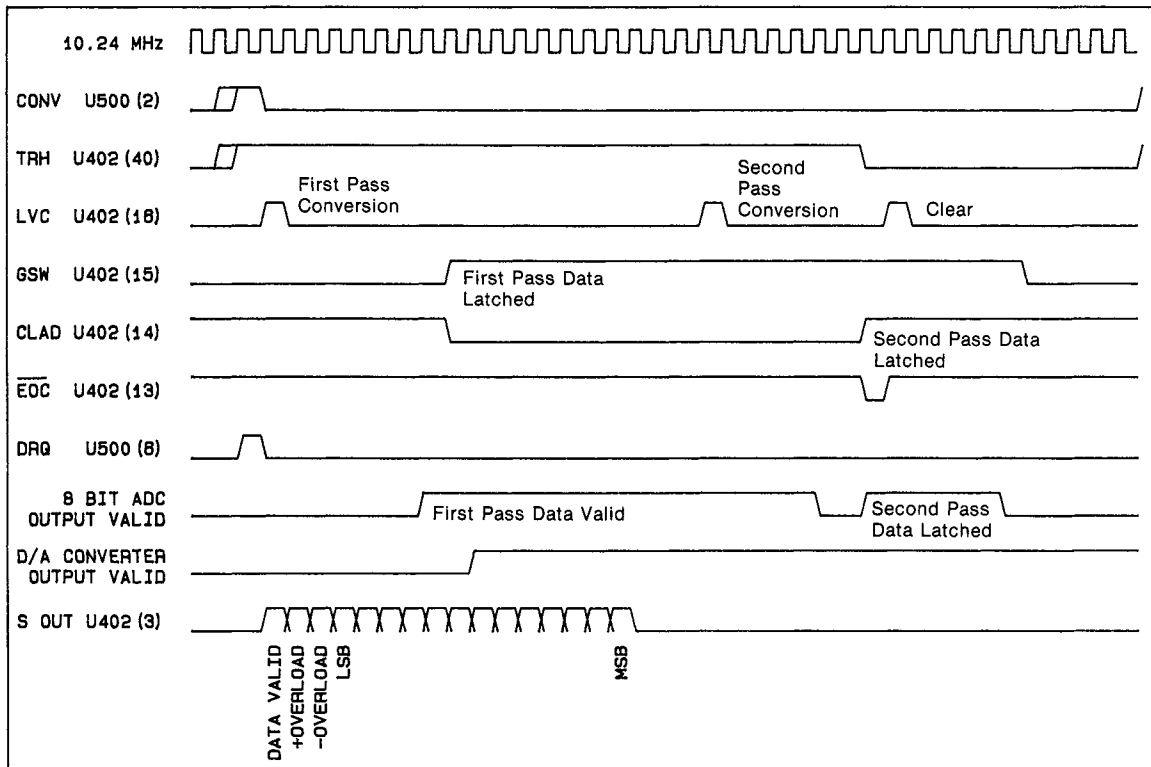
#### **[A] 100 kHz LOW PASS FILTER**

The 100 kHz low pass filter is a 4 stage filter with a gain of 0.557 and zeros at 371 kHz, 166 kHz, 151 kHz, and 214 kHz.

#### **[F] TIMING CONTROL ISOLATION INTERFACE, [N] DATA OUTPUT ISOLATION INTERFACE, [T] STATUS ISOLATION INTERFACE, [U] TRIGGER ISOLATION INTERFACE**

The isolation interface circuits use transformer coupling to isolate the floating ground from the chassis ground. Move the -hp-3561A front panel ground switch to the CHASSIS position to short the two grounds together. All of the transformer coupled interfaces are non-inverting.

**Figure 7-4 A/D Converter Signal Timing**



**[G] TRACK AND HOLD**

The track and hold circuit is controlled by the TRH signal generated in the ADC timing and control circuit. When the TRH signal is high, this circuit is an inverting unity gain amplifier. When the TRH signal goes low, the track and hold circuit samples the input signal and holds the sampled value until the TRH signal goes high again. The track and hold circuit samples the input data at a 256 kHz rate.

**[H] SECOND PASS ADC INPUT**

The Second Pass ADC input circuit consists of a 13 bit D/A converter, and a summing amplifier. The D/A converter outputs an analog signal which is equal to the first pass 8 bit ADC conversion. This signal is then subtracted from the actual track and hold output signal in U205 resulting in a signal which is equal to the error between the first pass 8 bit digital approximation, and the actual track and hold output. This error signal is multiplied by 32 and then input to the 8 bit ADC for the second pass conversion.

**[I] TEST REGISTER**

The test register is an extension of the front end control register on the A10 Assembly. The FEDATAIC signal is clocked into the register with the FECLKI signal. When the register is full the FELATCHI signal latches the data. The test register output programs the ADC timing and control circuit.

**[K] A/D INPUT SWITCH**

The A/D input switch selects which signal will be input to the 8 bit ADC. The GSW and CALD signals generated in the A/D timing and control circuit control the position of the ADC input switch as shown in Table 7-7.

**Table 7-7 ADC Input Switch Control**

GSW	CLAD	Input Selected
1	0	Second Pass Input
1	1	.34 Vdc Reference
0	0	First Pass Input
0	1	First Pass Input

**[L] A/D TIMING AND CONTROL**

The A/D timing and control circuit performs four major functions. First, the A/D timing and control circuit generates the control signals which coordinate the two passes of data through the 8 bit ADC, and control the track and hold circuit. Second, it transfers the first pass 8 bit ADC output to the D/A converter in the second pass input circuit. Third, it divides the second pass 8 bit ADC output by 32 and adds the result to the first pass 8 bit ADC output to obtain a final 13 bit result. Finally, the timing and control circuit transfers the 13 bit digital data to the digital filters on the A20 Assembly.

The digital filter on the A20 Assembly controls the A/D converter through the CONV and DRQ signals. The CONV signal is used to initiate an A/D conversion, and the DRQ signal is used to request the resultant data. Data is transferred to the digital filter with every DRQ, however, if the A/D conversion is not yet complete, the data will be invalid. The digital filter reads the DATA VALID bit of the transferred data to determine whether it should use the data or request the data again by sending another DRQ.

To improve the linearity of the A/D converter, the timing and control circuit adds 5 bits of noise to the first pass result, and then subtracts this noise back out of the second pass results.

**[O] ANALOG TO DIGITAL CONVERTER (8 BIT ADC)**

This circuit is a single chip 8 bit A/D converter. An analog to digital conversion is initiated on the rising edge of the LCV signal and data is valid 600 nSec later. The 8 bit ADC has an operating range of +0 volts to -1.0 volts.

**[P] OVER-RANGE/HALF-RANGE**

This circuit compares the input signal to a fixed voltage reference to generate the overload (OVL), and half-range (6dB+, 6dB-) signals. Comparator outputs are high when tripped by a fault condition.

**Table 7-8 A15 Assembly Signal Descriptions**

<b>Signal</b>	<b>Description</b>
CLAD	Clear 8 bit ADC: Selects a .34 Vdc signal as the input to the 8 bit ADC between the first and second pass conversions to clear the 8 bit ADC.
COMP	COMParE input: Identical to the main signal input from the A10 Assembly. This signal is used to generate HALFR, OVERR, and FETRIG.
CONV	CONVert: This signal initiates the two pass A/D conversion process.
DATAOUT	DATA OUTput: 13 bit serial data transferred to the digital filter LSB leading plus two bits to indicate overloads, and one bit to indicate data valid.
DRQ	Data ReQuest: Tells the A/D converter that the digital filter on the A20 Assembly is ready for new data.
EOC	End Of Conversion: Signifies that the two pass A/D conversion is complete.
<u>FECLKI</u>	Front End CLOCK: Clocks the FEDATA signal into the test register.
FEDATAIC	Front End DATA: Serial data which, when latched into the test register, programs the A/D timing and control circuit.
FELATCHI	Front End LATCH: Latches the FEDATA signal in the test register.
FETRIG	Front End TRIGger: Triggers a measurement when the instrument is in the input trigger mode.
GSW	Gate SWitch: Goes low to select the first pass ADC input circuit and goes high to select the second pass ADC input circuit.
HALFR	HALF-Range: Goes high when the input is more than 6 dB below the range setting.
LCV	Local ConVert: Initiates an A/D conversion in the 8 bit ADC. Two 8 bit ADC conversions and one clear are needed for each complete A/D conversion.
OVERR	OVER-Range: Goes high when the input signal is greater than 2.8 dB above the range setting.
OFERQ	Over-FREQuency: Goes high when the external sample frequency is greater than 256 kHz.
SSTAT	Serial STATus: Serial data which outputs the status of the HALFR, OVERR, OFREQ, and FEDATA signals to the digital filter.
TRH	TRack/Hold: Goes high to place the track and hold circuit in the track mode and low to place the track and hold circuit in hold mode.
TRIG LVL	TRIGger LeVeL: Sets the trigger level for the input trigger.

**[R] STATUS LATCH**

Three status bits are generated for each A/D data output, half-range (HALFR), over-range (OVERR), and over-frequency (OFREQ). HALFR is high when the input signal is between 0dB and 6dB below the range setting, and OVERR is high when the input

signal is greater than 2.8 dB over the range setting. OFREQ is high when the external sample frequency is greater 256 kHz. In addition, the status word contains one bit of the FEDATA signal. This allows the processor to read the front end programming data to verify proper programming. The status data is transferred to the digital filter when a data request (DRQ) signal is received.

## [S] TRIGGER LEVEL COMPARATOR

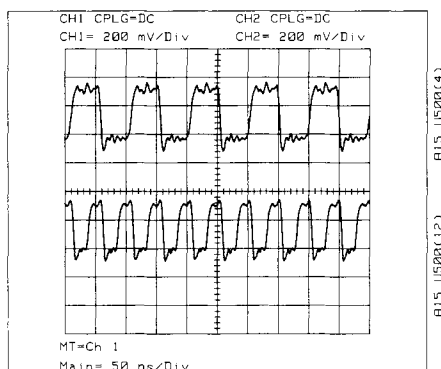
This circuit compares the input signal to the trigger level signal generated on the A10 Assembly. When the input signal exceeds the trigger level signal, the comparator output goes low. A trigger level of 100 % of range results in a  $1.29 \text{ Vdc} \pm .12 \text{ Vdc}$  signal at the TRIG LEV test point.

## 7-9 Troubleshooting the Digitizer

### GENERAL

Troubleshooting the A15 Assembly should be performed in two steps: analog troubleshooting and digital troubleshooting. The primary method for troubleshooting the analog circuitry is to input a sine wave into A15J1 and then check the signal at each of the analog circuit blocks. The primary method for troubleshooting the digital circuitry is to check the control signals against the timing diagram given in Figure 7-4. Move the front panel ground switch to the CHASSIS position and verify the 20.48 MHz and 10.24 MHz clocks shown in Figure 7-5 before troubleshooting this assembly.

**Figure 7-5 A15 Assembly Clock Waveforms**



Probe: 10:1

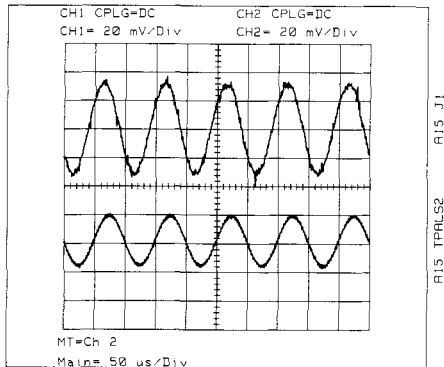
Ch1: Connection: A15U500(4) 10.24 MHz  
Coupling- dc  
Ground- Third Graticule From Top

Ch2: Connection- A15U500(12) 20.48 MHz  
Coupling- dc  
Ground- Third Graticule From Bottom

Trigger: Internal- Ch1  
Slope- Positive

Bandwidth limit: ON

Figure 7-6 A15 Assembly Analog Waveforms in Test 115



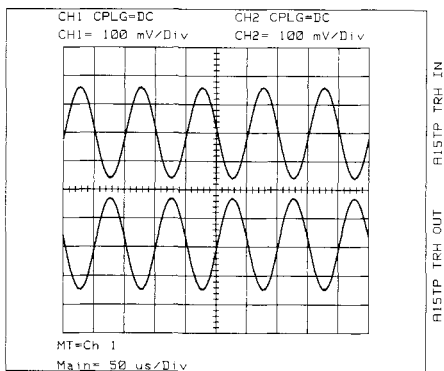
Probe: 10:1

Ch1: Connection: A15J1  
(.23 ± .01 Vrms)  
Coupling- dc  
Ground- Third Graticule From Top

Ch2: Connection- A15TP"ALS2"  
(.135 ± .006 Vrms)  
Coupling- dc  
Ground- Third Graticule From Bottom

Trigger: Internal- Ch2  
Slope- Negative

Bandwidth limit: ON



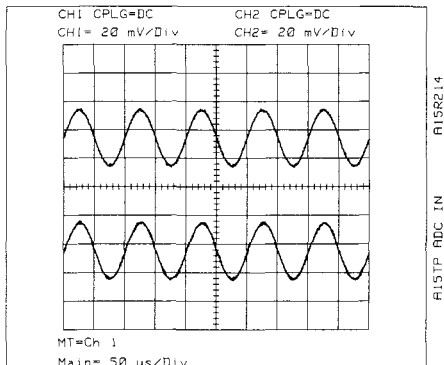
Probe: 10:1

Ch1: Connection- A15TP"TRH IN"  
(1.1 Vrms)  
Coupling- dc  
Ground- Third Graticule From Top

Ch2: Connection- A15TP"TRH OUT"  
(1.1 Vrms)  
Coupling- dc  
Ground- Third Graticule From Bottom

Trigger: Internal- Ch1  
Slope- Positive

Bandwidth Limit: ON



Probe: 10:1

Ch1: Connection- A15 R214  
(.14 ± .01 Vrms)  
Coupling- dc  
Ground- Second Graticule From Top

Ch2: Connection- A15TP"ADC IN"  
(.14 ± .01 Vrms)  
Coupling- dc  
Ground- Fourth Graticule From Bottom

Trigger:- Internal- Ch1  
Slope- Positive

Bandwidth Limit: ON

**[A] 100 kHz LOW PASS FILTER, [B] X3 AMPLIFIER, [C] 482 kHz LOW PASS FILTER, [D] X3 AMPLIFIER, [G] TRACK AND HOLD, [H] SECOND PASS ADC INPUT, [M] ADC INPUT BUFFER**

To check these circuits, set the -hp-3561A controls as follows:

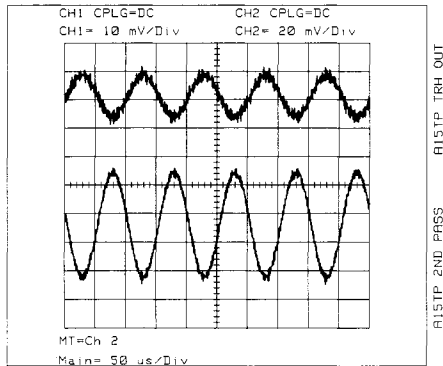
```

PRESET
RANGE ..... DEFINE RANGE .....0 dBV
MODE ..... TEST SELECT.....DEFINE TST NUM .....115 ENTER
                        START SNGL TST
    
```

In this test the TRH signal is held low, causing the track and hold circuit to operate as a unity gain inverting amplifier. In addition, Test 115 programs the ADC input switch to select the first pass ADC input circuit as the input path to the 8 bit ADC.

1. Remove cable W15 from A15J1. Use the frequency synthesizer and a BNC to SMB adapter cable to input a .228 Vrms, 11 kHz sine wave into A15J1. Terminate the frequency synthesizer with 50 Ω.
2. Verify the waveforms shown in Figure 7-6. The signals shown in the figure are listed in the order of signal flow.
3. If all the signals in Figure 7-6 are correct, reduce the amplitude of the input sine wave to 10 mVrms, and verify the signals as shown in Figure 7-7. In Test 115, the output of the D/A converter (U102) is set to zero.

**Figure 7-7 Second Pass ADC Input Waveforms In Test 115**



Probe: 10:1

Ch1: Connection- A15TP"TRH OUT"  
 (15 ±1 mVrms)  
 Coupling- dc  
 Ground- Second Graticule From Top

Ch2: Connection- A15TP"2ND PASS"  
 (55 ±3 mVrms)  
 Coupling- dc  
 Ground- Center Graticule

Trigger: Internal- Ch2  
 Slope- Positive

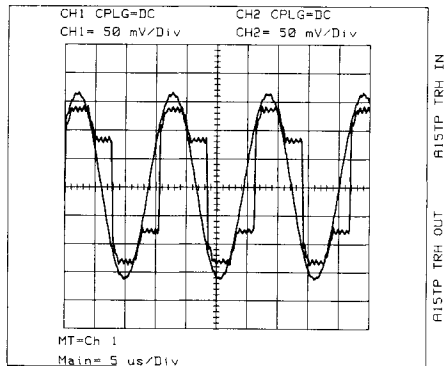
Bandwidth Limit: OFF

**[G] TRACK AND HOLD**

To check the track and hold circuit for proper operation, press the -hp-3561A PRESET key. When the preset is complete, use a frequency synthesizer, and a BNC to SMB adapter cable to input a 64 kHz, .228 Vrms sine wave into A15J1. Terminate the frequency synthesizer with 50 Ω. Check the TRH IN and TRH OUT test points for

the waveforms shown in Figure 7-8 to verify that the track and hold circuit is sampling the sine wave. Check for excessive DC offset or overshoot of the sampled signal. If there appears to be a problem in the track and hold output signal, check the TRH and FETG signals for the waveforms shown in Figure 7-8.

**Figure 7-8 Track and Hold Waveforms**



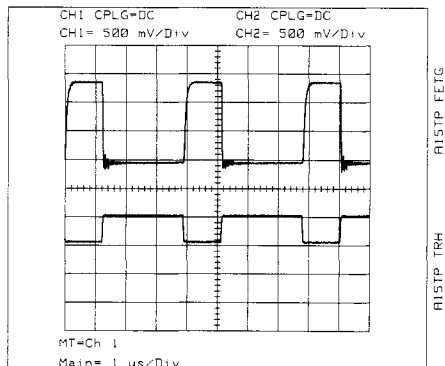
Probe: 10:1

Ch1: Connection- A15TP"TRH IN"  
Coupling- dc  
Ground- Center Graticule

Ch2: Connection- A15TP"TRH OUT"  
Coupling- dc  
Ground- Center Graticule  
Invert Ch2

Trigger: Internal- Ch1  
Slope- Positive

Bandwidth Limit: ON



Probe: 10:1

Ch1: Connection- A15TP"FETG"  
Coupling- dc  
Ground- Third Graticule From Top

Ch2: Connection- A15TP"TRH"  
Coupling- dc  
Ground- Third Graticule From Bottom

Trigger: Internal- Ch1  
Slope- Positive

**NOTE**

*Adjust the frequency of the frequency synthesizer to within .5 Hz of 64 kHz to stabilize the waveform.*

**TROUBLESHOOTING DISTORTION**

Distortion may be isolated to either the 100 kHz filter and X3 amplifiers, or the track and hold and A/D converter circuits. Use a low distortion oscillator, which meets the required characteristics listed in Table 1-5, when making any distortion or noise measurements.



1. Press the -hp-3561A PRESET key. When the preset is complete, use the low distortion oscillator and a BNC to SMB adapter cable to input an 11 kHz, 0.228 Vrms sine wave into A15J1. Terminate the low distortion oscillator in 600 Ω. If any of the harmonics are less than 80 dB below the 11 kHz fundamental, proceed with step 2.
2. Remove jumper J100 on the A15 Assembly, and input a 11 kHz, 1.14 Vrms (1.61 Vpeak) sine wave into the TRH IN test point. This removes circuit blocks A through D from the signal path.

If any of the harmonics are less than 80 dB below the 10 kHz fundamental, the distortion failure is most likely in the track and hold circuit or the A/D converter.

If all of the harmonics are now greater than 80 dB below the 10 kHz fundamental, the distortion failure is most likely in the 100 kHz low pass filter or the X3 amplifiers.

**[F] TIMING AND CONTROL ISOLATION INTERFACE, [L] ADC TIMING AND CONTROL**

To check these circuits, press the -hp-3561A PRESET key, and verify the control signals as shown in Figure 7-4.

**[N] DATA OUTPUT ISOLATION INTERFACE**

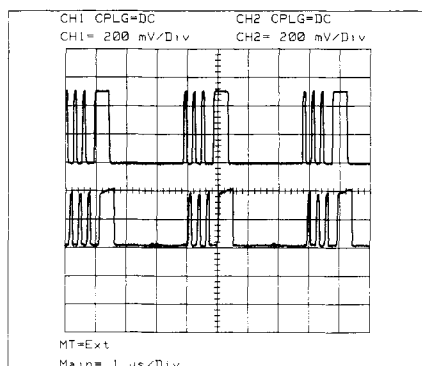
To check this circuit, set the -hp-3561A controls as follows:

```

PRESET
RANGE ..... DEFINE RANGE ..... 0 dBV
MODE ..... TEST SELECT ..... DEFINE TEST NUM ..... 112 ENTER
START SNGL TST
    
```

In this test, the timing and control circuit outputs a test pattern as shown in Figure 7-9.

**Figure 7-9 Test pattern Output in Test 112**



```

Probe: 10:1
Ch1: Connection- A15U402(3)
Coupling- dc
Ground- Fourth Graticule From Top
Ch2: Connection- A15U406(6)
Coupling- dc
Ground- Third Graticule From Bottom
Trigger: External- A15TP"DRQ"
Slope- Positive
Bandwidth Limit: ON
    
```

**BREAKING THE SECOND PASS FEEDBACK LOOP**

Test 113 is provided to isolate failures to either the first pass circuit or the second pass circuit. To initiate this test, set the -hp-3561A controls as follows:

```

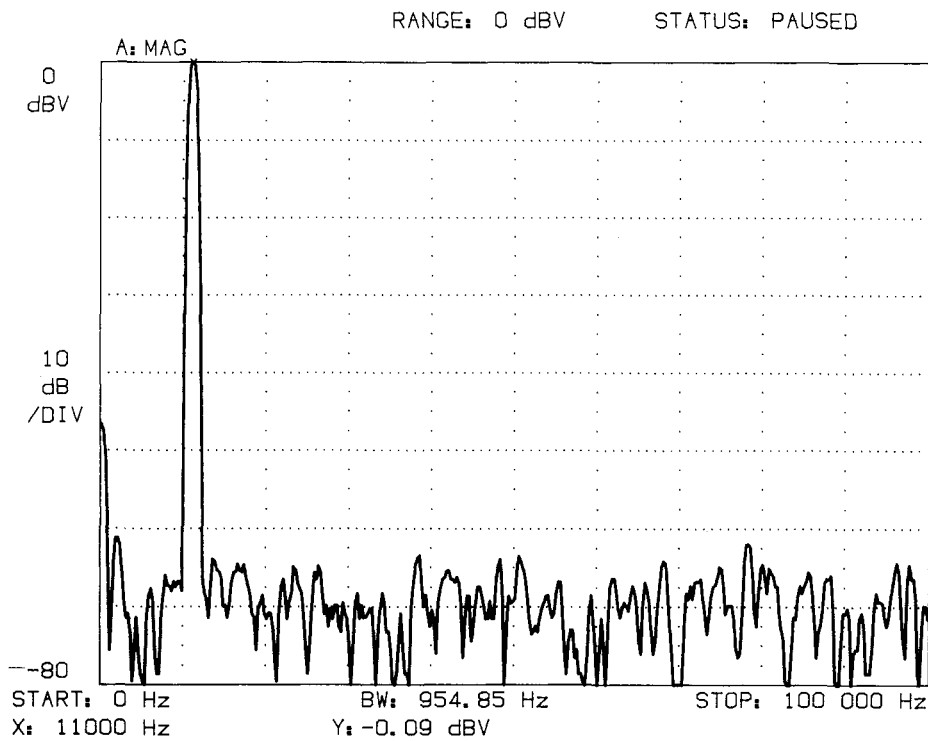
PRESET
FORMAT ..... SINGLE
RANGE ..... DEFINE RANGE .....0 dBV
MODE ..... TEST SELECT .....DEFINE TEST NUM .....113 ENTER
                        START SNGL TST
    
```

When the "TEST #113 IS COMPLETE" message is displayed, press the MODE key. In this test, data is not passed through the second pass ADC input circuit, thus, if a failure appears, it is most likely in the 8 bit ADC, or the timing and control circuit. Use the frequency synthesizer and a BNC to SMB adapter cable to input an 11 kHz, .228 Vrms sine wave into A15J1. Terminate the frequency synthesizer in 50 Ω. Check the -hp-3561A display for a full scale sine wave as shown in Figure 7-10.

**NOTE**

*Because the second pass circuit is not operating, noise and harmonics will be 50 to 70 dB below the amplitude of the 11 kHz fundamental. The test is failing if either the noise or harmonics are less than 50 dB below the fundamental.*

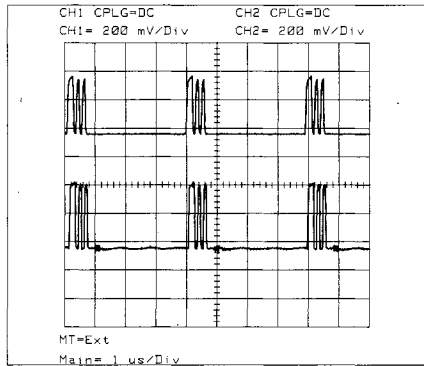
**Figure 7-10 -hp-3561A Display in Test 113**



**[R] Status Latch, [T] Status Isolation Interface**

To check these circuits, press the -hp-3561A PRESET key, disconnect the input signal, and verify the waveforms shown in Figure 7-11.

**Figure 7-11 A15 Status Output**



Probe: 10:1

Ch1: Connection: A15TP"SSST"  
Coupling- dc  
Ground- Third Graticule From Top

Ch2: Connection: A15TP"SSSTAT"  
Coupling- dc  
Ground- Third Graticule From Bottom

Trigger: External- A15TP"DRQ"  
Slope- Positive

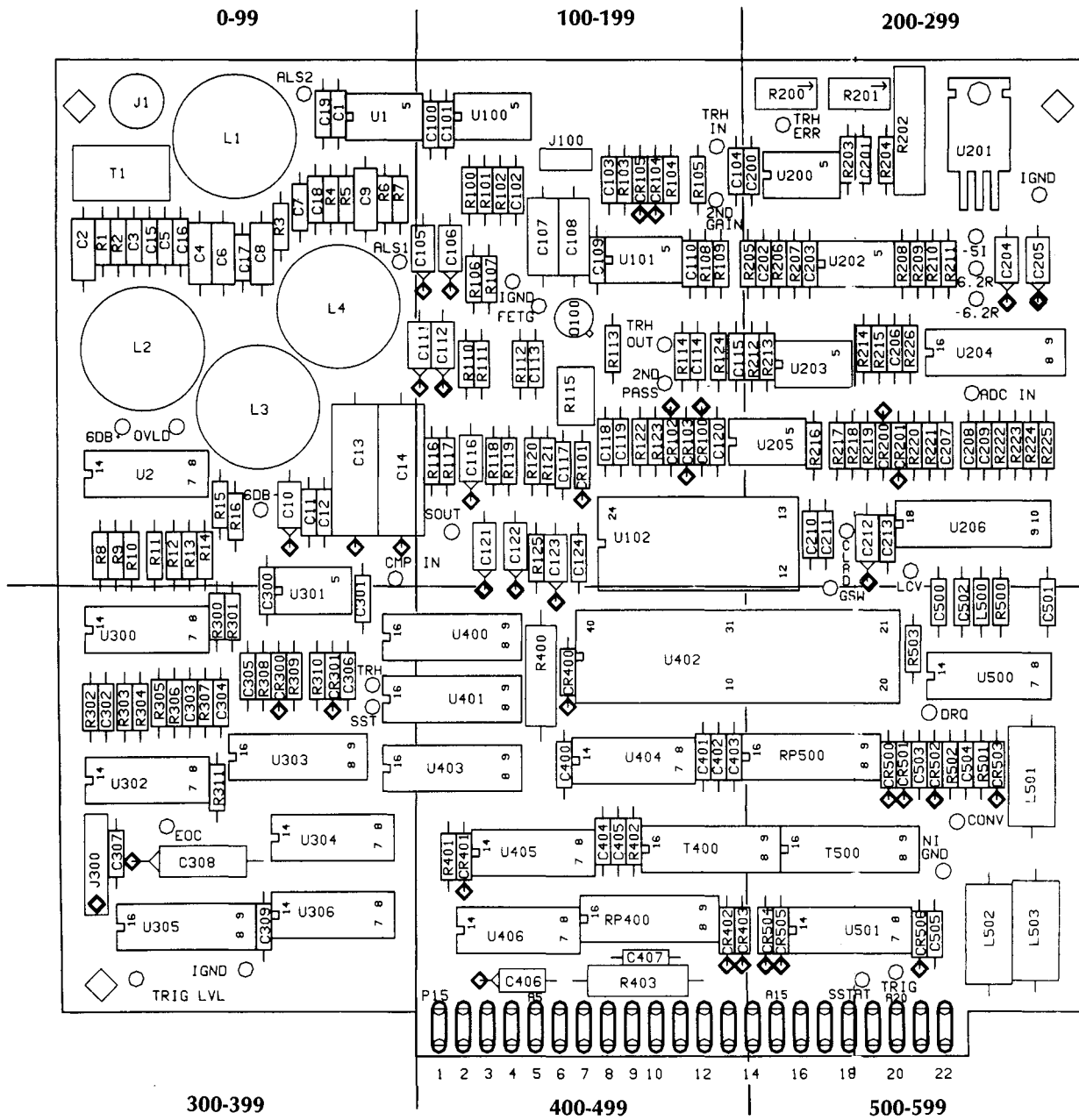
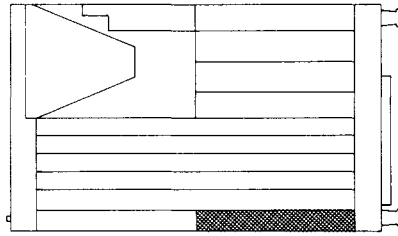
**Table 7-9 A15 Assembly Signal Connections**

**INPUTS**

Signal Name	Functional Block	Connector Number	Origin Assembly
COMP	Q	P15(B1)	A10
CONVERT	F	P15(B16)	A20
DATA REQ	F	P15(B14)	A20
FECLOCK	I	P15(A2)	A10
FEDATA	I	P15(A1)	A10
FELATCH	I	P15(A3)	A10
ISM	L	P15(A6)	A20
SIGNAL INPUT	A	J1	A10
TRIGLVL	S	P15(B2)	A10
10 MHz	F	P15(A15)	A20
20 MHz	F	P15(B15)	A40

**OUTPUTS**

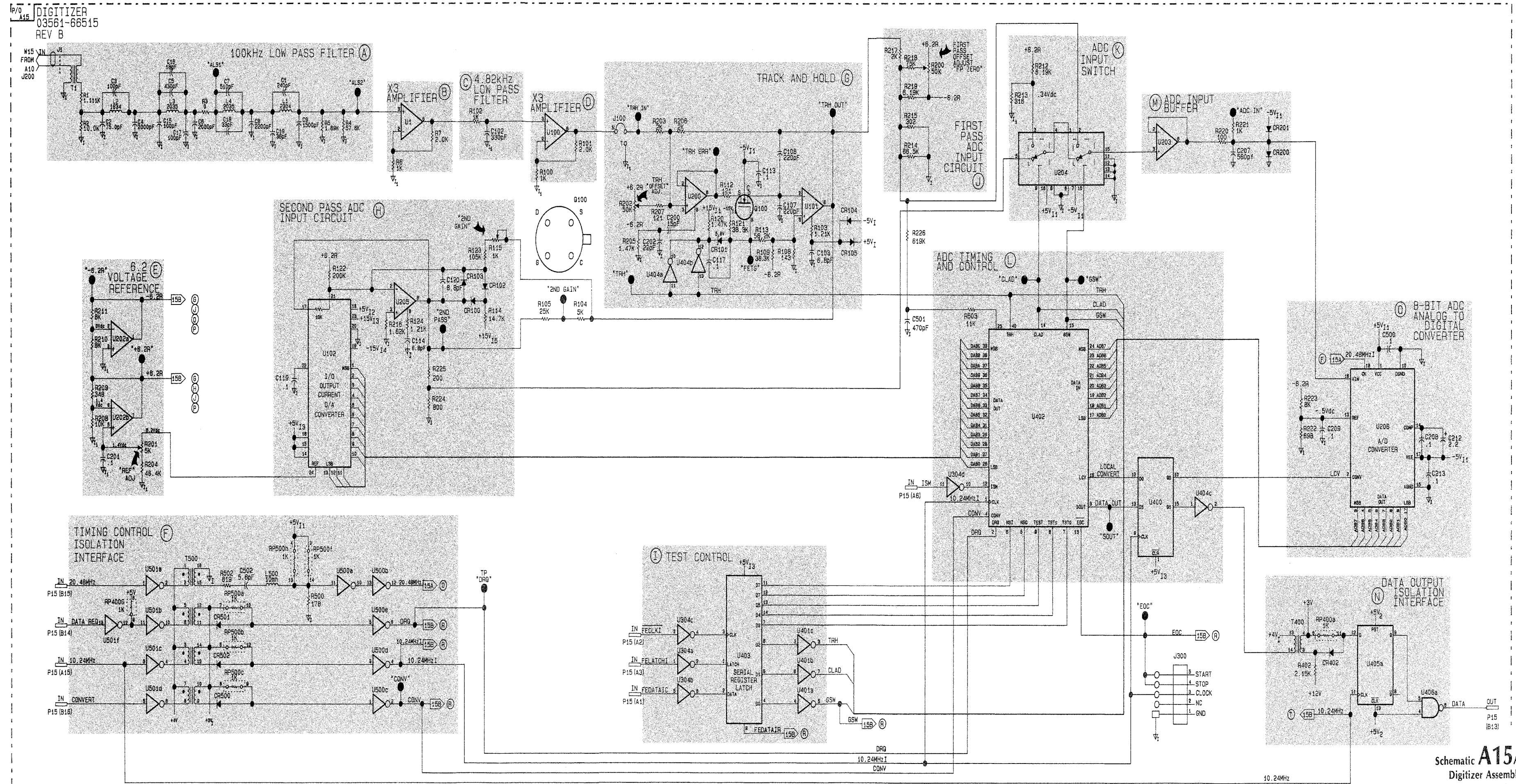
Signal Name	Functional Block	Connector Number	Destination Assemblies
SSTAT	T	P15(A14)	A20
FETRIG	U	P15(A13)	A20
A/D DATA	N	P15(B13)	A20



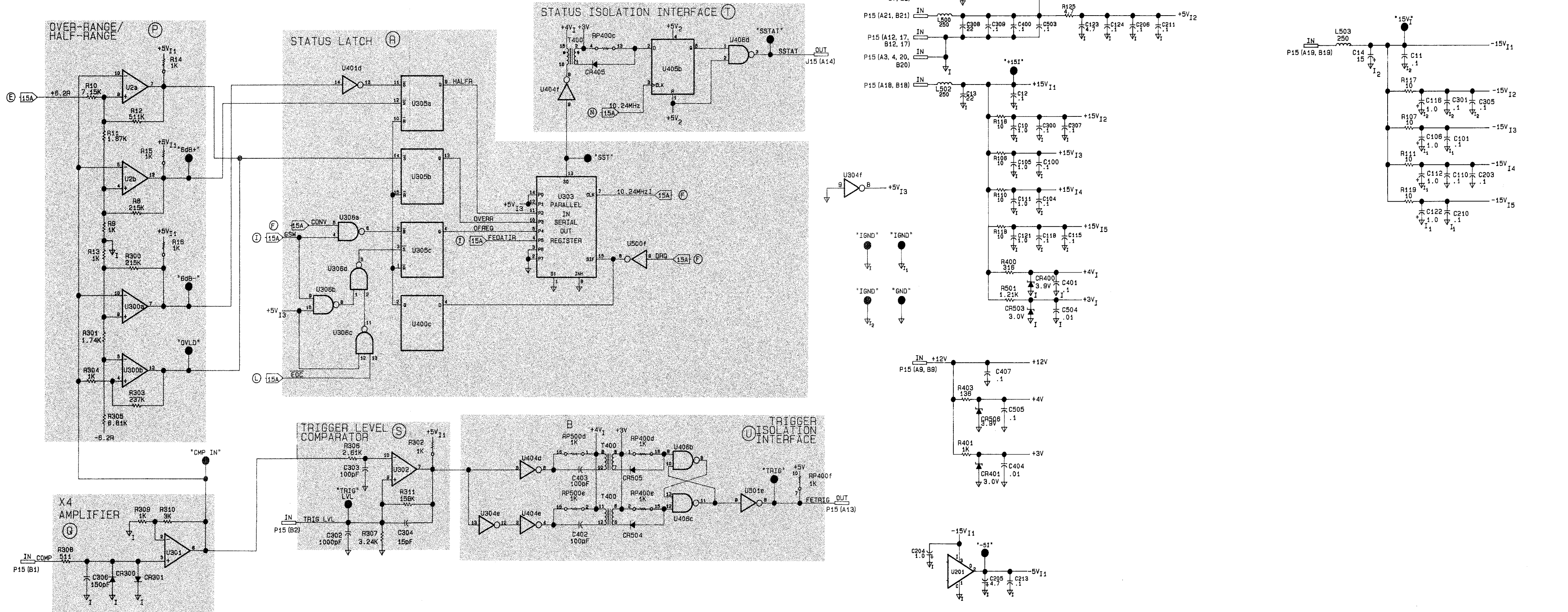
A15 Assembly

	+15V <sub>12</sub>	+15V <sub>13</sub>	+15V <sub>14</sub>	+15V <sub>15</sub>	-15V <sub>12</sub>	-15V <sub>13</sub>	-15V <sub>14</sub>	-15V <sub>15</sub>	+5V <sub>1</sub>	+5V <sub>12</sub>	-5V <sub>1</sub>	GND <sub>1</sub>
U1	11	7			6	4						
U2	11	7			6	4						
U100												
U101	7	7										
U102			23				4	19				18
U200							4					
U201												
U202												
U203												
U204										7		16
U205												
U206										1		17
U300	11				6							
U301	7				4							
U302	11				6							
U303												16
U304												14
U305												16
U306												14
U400												16
U401												16
U402												30
U403												16
U404												14
U500												14

	+5	GND
U405	14	7
U406	14	7
U501	14	7







## **7-10 A20 DIGITAL FILTER ASSEMBLY**

### **7-11 Digital Filter Circuit Description**

#### **GENERAL**

The primary purpose of the digital filter is to provide anti-alias filtering when the -hp-3561A frequency span is less than 100 kHz. The digital filter receives input data from the A/D converter, it then processes the data and stores the results directly into the instrument RAM. Other circuits on the A20 Assembly include the timing and control counter, the A/D converter interface, and the direct memory access (DMA) counters which interface the digital filter with the instrument RAM.

#### **DIGITAL FILTER CHANNEL DESCRIPTIONS**

The digital filter can store output data into two independent 1024 data point buffers in RAM, channel R, and channel G. Addressing is accomplished through the channel R and channel G direct memory access (DMA) counters. Each channel is set to one of three data modes. The data mode for a channel defines what type of data is transferred from the digital filter into RAM on that channel. In mode one, the digital filter outputs "real part" data (filtered by U1 only); in mode two, the digital filter outputs "imaginary part" data (filtered by U401 only); and in mode three, the digital filter outputs unfiltered A/D data directly. More than one type of data can be stored in a channel at the same time (e.g., in zoom mode, 512 real part and 512 imaginary part data samples are stored in channel G). Table 7-10 lists the data mode settings for each -hp-3561A measurement mode.

#### **[B] CHANNEL R DMA COUNTER, [D] CHANNEL R ADDRESS BUS LATCH**

The output of this counter defines the address in RAM where channel R data is stored. The channel R bus grant signal latches the counter output onto the RAM address bus, and increments the counter by one. The channel R counter clocks through 1024 positions and then issues a DONER signal to indicate that the channel R buffer in RAM has been filled and is ready to be processed by the FFT processor.

#### **[C] CHANNEL G DMA COUNTER, [E] CHANNEL G ADDRESS BUS LATCH [L] CHANNEL G COUNTER PRESET**

The output of this counter defines the address in RAM where channel G data is stored. The channel G bus grant signal latches the counter output onto the RAM address bus and increments the counter by one. The channel G DMA counter clocks through up to 40,960 positions before a DONEG signal is issued. The exact number is programmed by the central processor through the channel G preset circuit.

**[H] DMA CONTROL LATCH, [J] DMA CHANNEL CONTROL**

Through this register, the central processor programs the data mode for channel R and channel G, the number of counts for the channel G DMA counter, the trigger state, and the digital filter test mode. On the falling edge of the DIS1-3 signals, the digital filter processes one time record (1024 data points).

**[I] RAM BUS INTERFACE, [K] DMA CHANNEL SELECT**

The digital filter issues a RAM bus request whenever it is ready to store a data point in RAM. The particular bus request issued depends on the data mode the digital filter is operating in. When the digital filter receives a bus grant from RAM, the DMA channel select circuit issues a bus grant to the selected DMA counter, which then transfers the data onto the RAM data bus.

**[M] DIGITAL FILTER**

The digital filter consists of three integrated circuits, U1, U4, and U401. The actual digital filtering occurs in U1 and U401, which are identical and interchangeable. The digital filter control circuit, U4, is primarily an interface and data selector. The digital filter receives three data inputs: A/D DATA and the local oscillator inputs, COSINE, and -SINE. The local oscillator inputs which are only active during zoom operation are multiplied with the A/D DATA signal within the digital filter. The digital filter control circuit, based on the -hp-3561A front panel settings, selects the type of data (mode one, mode two or mode three) which is output to the RAM data bus. Table 7-10 lists which digital filter ICs are active in each -hp-3561A measurement mode.

**Table 7-10 Digital Filter Operation**

<b>-hp-3561 Front Panel Setting</b>	<b>Digital Filter Circuits in Use</b>	<b>Channel G Data Mode</b>	<b>Channel R Data Mode</b>
Baseband -Magnitude -Phase -Time	U4, U1	1	not used
Zoom -Magnitude -Phase -Time	U4, U1, U401	1	not used
Third Octave	U4, U1, U401	1	2
Full Octave	U4, U1, U401	1	2
Input Time	U4	not used	3
Input Magnitude	U4	not used	3



**[O] A/D STATUS LATCH, [Q] DATA REQUEST/SYNC2 SIGNAL GENERATOR [U] DIGITAL FILTER INPUT DATA LATCH**

These circuits comprise the A/D converter and local oscillator interface. To initiate an A/D data transfer, the digital filter issues a SHIFT1 signal which triggers a  $\overline{\text{DATA REQ}}$  signal. On receipt of a  $\overline{\text{DATA REQ}}$  signal, the A/D converter transfers one 13 bit data sample into the digital filter through the digital filter input data latch, and one 4 bit status word into the digital filter through the A/D status latch. If the A/D does not yet have a new data sample, it will transfer invalid data. The digital filter reads the first bit of the A/D data to determine if the data is valid. If the data is invalid, the digital filter will continue to request data at a 512 kHz rate. When valid data is received, the digital filter will continue to request new data samples at a 256 kHz rate.

For each valid A/D data sample received, the digital filter issues a SYNC2 signal, which is a data request to the local oscillator. On receipt of a SYNC2 signal, the local oscillator transfers one 16 bit COSINE value and one 16 bit -SINE value to the digital filter.

**[P] CONVERT SIGNAL TIMING, [T] CONVERT SIGNAL SELECT**

The CONVERT signal establishes the sampling rate of the -hp-3561A. On receipt of a CONVERT signal, the A/D converter samples the input data and initiates an A/D conversion. In internal sample mode, the  $\overline{\text{DATA REQ}}$  signal is selected to trigger a CONVERT pulse and in external sample mode, the rear panel "EXT SAMP" input is selected to trigger a CONVERT pulse.

**[Y] TIMING AND CONTROL COUNTER, [X] COUNTER CLOCK SELECT [V] TRIGGER TIMING, [W] PHASE COUNTER CLOCK**

All of these circuits provide inputs to the multi-function counter, U202. The multi-function counter contains six counters which can each be programmed to use any one of the four clock inputs. The central processor programs the multi-function counter to determine the timing relationship between the various activities within the -hp-3561A. It then uses this information to calculate phase corrections for the input signal.

**[CC] CAL SIGNAL/TRIGGER CONTROL [EE] TRIGGER SELECT, [DD] CAL SIGNAL SELECT**

Through these circuits, the central processor programs the correct trigger and calibration signal for the current front panel setting. The resulting trigger signal, NSTRIG, is synchronized to the internal 10.24 MHz clock in the trigger timing circuit, and used to trigger a measurement.

**Table 7-11 A20 Assembly Signal Descriptions**

<b>Signal</b>	<b>Description</b>
BGG	RAM Bus Grant channel G: Clocks the channel G DMA counter output onto the RAM address bus and increments the counter by one.
BGR	RAM Bus Grant channel R: Clocks the channel R DMA counter output onto the RAM address bus and increments the counter by one.
BREN	Bus Request ENable: Enables the channel G bus request signal to be input to the multi-function counter.
CAL GEN	CALibration signal GENerator: A square wave with a frequency programmed by the central processor (4 kHz when the front panel cal signal is selected).
CAL TRIG	CALibration signal TRIGger: Triggers a measurement at the start of the PRN cal signal.
CHGCNT	CHannel G CouNT: Used by the central processor to read the position of the channel G DMA counter over the RAM address bus.
CLRTRIG	CLear TRIGger: Clears the current instrument trigger state.
CONVERT	A/D CONVERT: Initiates a data sample in the A/D converter and establishes the instrument sample rate.
CTRRS	CounTeR Read Select: Used by the central processor to read data from the multi-function counter.
CTRWS	CounTeR Write Select: Used by the central processor to write programming data to the multi-function counter.
DATA REQ	A/D DATA REQuest: Causes the A/D converter to transfer its current data to the digital filter.
DF1BC	Digital Filter 1-3 Bus Grant: RAM bus grant for data mode one, two, or three.
DF2BC	
DF3BC	
DF1BR	Digital Filter 1-3 Bus Request: RAM bus request for data mode one, two, or three.
DF2BR	
DF3BR	
DFIS1	Digital Filter Input Status: Used by the processor to address the digital filter status word.
DFOS1	Digital Filter Data Strobe: Used by the processor to load data directly from the RAM data bus into the digital filter for processing (data mode one, two, or three).
DFOS2	
DFOS3	
DIS1	DISable data mode 1-3: Disables data mode one, two, or three in the digital filter.
DIS2	
DIS3	
DONEG	DONE with channel G count: Triggers a DMA interrupt to the central processor to indicate that the channel G RAM buffer is full.
DONER	DONE with channel R count: Triggers a DMA interrupt to the central processor to indicate that the channel R RAM buffer is full.
EXTSAMP	EXTernal SAMPlE clock: Rear panel external sample input signal.
FECLK	Front End CLock: Clocks the FEDATA signal into the front end control register on the A10 Assembly.

**Table 7-11 A20 Assembly Signal Descriptions (Cont'd)**

Signal	Description												
FEDATA	Front End Data: Data to program the relays and other circuits on the A10 and A15 Assemblies.												
$\overline{\text{FECS}}$	Front End Control Select: Clocks data into the front end control latch and the cal signal/trigger select circuits.												
FELATCH	Front End LATCH: Latches the front end data into the front end control register on the A10 Assembly.												
G0S, G1S	Channel G Data Mode Select: <table border="0"> <tr> <td>Data Mode</td> <td>G0S</td> <td>G1S</td> </tr> <tr> <td>Mode 1</td> <td>0</td> <td>0</td> </tr> <tr> <td>Mode 2</td> <td>0</td> <td>1</td> </tr> <tr> <td>Mode 3</td> <td>1</td> <td>0</td> </tr> </table>	Data Mode	G0S	G1S	Mode 1	0	0	Mode 2	0	1	Mode 3	1	0
Data Mode	G0S	G1S											
Mode 1	0	0											
Mode 2	0	1											
Mode 3	1	0											
HALFR	HALF Range: Input Signal is between 0 dB and 6 dB below the range setting.												
OFREQ	Over FREQUENCY: External sample frequency is greater than 256 kHz.												
OVERR	OVER Range: Input signal is greater than 2.8 dB above the range setting.												
R0S, R1S	Channel R Data Mode Select: <table border="0"> <tr> <td>Data Mode</td> <td>R0S</td> <td>R1S</td> </tr> <tr> <td>Mode 1</td> <td>0</td> <td>0</td> </tr> <tr> <td>Mode 2</td> <td>0</td> <td>1</td> </tr> <tr> <td>Mode 3</td> <td>1</td> <td>0</td> </tr> </table>	Data Mode	R0S	R1S	Mode 1	0	0	Mode 2	0	1	Mode 3	1	0
Data Mode	R0S	R1S											
Mode 1	0	0											
Mode 2	0	1											
Mode 3	1	0											
$\overline{\text{SETTRIG}}$	SET TRIGger: Used by the processor to trigger a measurement when the -hp-3561A is set to internal trigger.												
SSTAT	A/D Serial STATus: 4 bit serial data which indicates the status of the current A/D DATA signal. SSTAT is transferred to the digital filter when a $\overline{\text{DATA REQ}}$ signal is received by the A/D converter.												
SYNC2	Issued by the digital filter to request data from the local oscillator.												

## 7-12 Troubleshooting the A20 Assembly

### GENERAL

Troubleshoot the circuits on the A20 Assembly in the order given in Table 7-12. In this table, level one circuits must be operational before level two circuits can be tested, and so on. Table 7-13 list some failure symptoms and the most likely cause of the failure. In addition, Table 7-14 lists all of the return codes for diagnostic self tests 13, 14, and 18. With the return code is given an error description and the most likely cause of the error. For the return code descriptions to be accurate, the diagnostic self tests should be run in numerical order.

**Table 7-12 A20 Troubleshooting Order**

Level	Functional Blocks
1	Clocks: FF GG
2	Processor Address Decoder: F
3	Processor Data Latch: S H N CC
4	Counter Clocks and Cal Signal Generator: V X AA
5	Timing and Control Counter: W Y Z DD EE
6	Digital Filter and Channel R DMA Counter: B D I K M
7	DMA Counters: C E G L
8	CONVERT Signal Timing: P Q T

**Table 7-13 A20 Failure Symptoms**

Symptom	Most Likely Cause of Failure
Instrument operates incorrectly in Input Time or Input Magnitude measurements only.	B Channel R DMA Counter
Instrument operates correctly in Input Time or Input Magnitude measurements only.	C Channel G DMA Counter Y Timing and Control Counter
Instrument operates incorrectly in zoom mode only.	U4 or U401

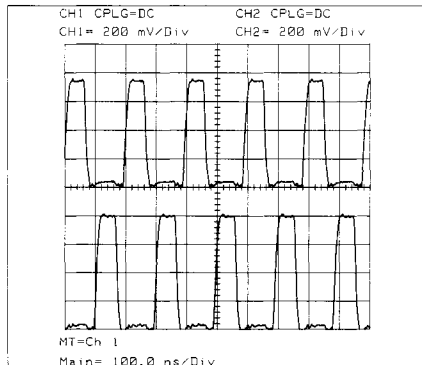
Table 7-14 A20 Diagnostic Test Return Code Descriptions

Return Code	Description	Most Likely Cause of Error
13 1 00 through 13 1 05	The processor is unable to program the timing and control counter.	U202 or U600, U300
13 6 00 through 13 6 02	The timing and control counter returns incorrect data.	U202 or X Counter Clock Select V Trigger Timing
14 2 00 through 14 2 02	The channel R DMA counter has not requested a data transfer in the allotted time.	B Channel R DMA Counter K DMA Channel Select I RAM Bus Interface or U1, U4, U401
14 2 03 through 14 2 10	The channel R DMA counter has not requested a data transfer in the allotted time.	U1 or U4: Odd numbered error code. U401 or U4: Even numbered error code.
14 5 00 through 14 5 10	The digital filter indicates a data overload.	U1 or U4: Odd numbered error code, or error code 00. U401 or U4: Even numbered error code.
14 6 00 through 14 6 02	Incorrect Data transferred to RAM.	B Channel R DMA Counter or U1, U4, U401
14 6 03 through 14 6 10	Incorrect Data transferred to RAM.	U1 or U4: Odd numbered error code. U401 or U4: Even numbered error code.
14 2 11 14 5 11 14 6 11	Data Incorrect or overload in zoom mode only.	U4
18 1 01 through 18 1 06	Timing and control counter error.	U202
18 3 01 through 18 3 07 Y	Incorrect Trigger.	J DMA Channel Control W Phase Counter Clock Timing and Control Counter
18 5 01	Digital filter indicates a data overload.	U1, U4, U401
18 9 01 through 18 9 04 or 18 6 01 18 6 02	Channel G DMA address error.	C Channel G DMA counter E Channel G Address Bus
18 8 00 through 18 8 15	Channel G DMA address error when using the channel G counter preset circuit.	E Channel G Address Bus L Channel G Counter Preset

**[FF] CLOCK GENERATOR, [GG] LOW FREQUENCY CLOCK GENERATOR**

Verify the clock waveforms with the waveforms given in Figure 7-12. The other clock signals can be checked against the frequencies listed on the schematic.

**Figure 7-12 A20 Clock Waveforms**



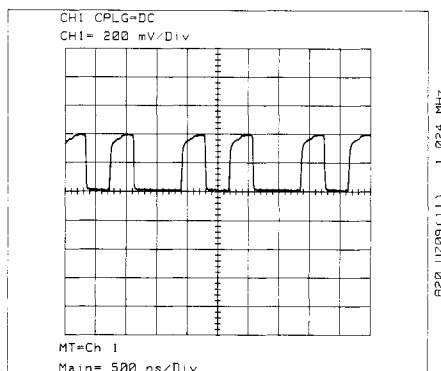
Probe: 10:1

Ch1: Connection- A20 TP1 "DFCLKφ2"  
Coupling- dc  
Ground- Center Graticule

Ch2: Connection- A20 TP102 "DFCLKφ1"  
Coupling- dc  
Ground- Bottom Graticule

Trigger: Internal- Ch1  
Slope- Positive

Bandwidth Limit: OFF



Probe: 10:1

Ch1: Connection- A20 U709(11) "1.024 MHz"  
Coupling- dc  
Ground- Center Graticule

Trigger: Internal- Ch1  
Slope- Positive

Bandwidth Limit: ON




**[F] PROCESSOR I/O ADDRESS DECODING, [H] DMA CONTROL LATCH  
[N] DIGITAL FILTER DATA BUS LATCH, [S] FRONT END CONTROL LATCH  
[CC] CAL SIGNAL/TRIGGER CONTROL**

1. Turn the -hp-3561A LINE power switch OFF.
2. Move jumper A40W1 on the A40 Assembly to the test position, and place the A20 Assembly on an extender board.
3. Turn the -hp-3561A LINE power switch ON.
4. When the "BLT TEST ROUTINE" message is displayed on the CRT screen, check the signatures given in Table 7-15.

**NOTE**

*The A60 Assembly may be removed during this test to disable the beeper, however, this also disables the display so the "BLT TEST ROUTINE" message will not be displayed. The signatures will be valid when the front panel LEDs begin to blink.*

**Table 7-15 A20 Processor Interface Signatures**

<b>Signature Analyzer Setup</b>			
<b>Signal</b>	<b>Polarity</b>	<b>Connection</b>	
Clock		A20J200(3) "RIOS"	
Start		A40J100(5)	
Stop		A40J100(4)	
+ 5 V Signature - H7PC			
<b>Processor I/O Address Decoding</b>		<b>DMA Control Latch</b>	
U106(6)	1590	U501(2)	0 volts
U306(7)	400C	U501(5)	0 volts
U306(9)	P86U	U501(6)	C829
U306(10)	PHPP	U501(9)	C829
U306(11)	571U	U501(12)	32F5
U306(12)	F4H9	U501(15)	6UF2
U306(15)	8HFP	U501(16)	0 volts
		U501(19)	0 volts
U307(7)	5250	U506(2)	6UF2
U307(9)	4712	U506(5)	5H07
U307(12)	PH40	U506(6)	32F5
U307(13)	18CU	U506(9)	32F5
U307(14)	962P	U506(12)	P52P
U307(15)	C068	U506(15)	P52P
		U506(16)	5H07
		U506(19)	32F5
<b>Front End Control Latch</b>		<b>Cal Signal Trigger Control</b>	
U510(2)	5A72	U509(2)	5C31
U510(5)	5C31	U509(3)	8FHA
U510(6)	5C31	U509(7)	8FHA
U510(9)	H6A8	U509(10)	0143
U510(12)	H6A8	U509(15)	H6A8
U510(15)	0143		
U510(16)	+ 5 volts		
U510(19)	8H99		
<b>Counter Data Bus Latch</b>			
U600(11)	4746		
U600(12)	7PHA		
U600(13)	4746		
U600(14)	PCFU		
U600(15)	4746		
U600(16)	H253		
U600(17)	PCFU		
U600(18)	PCFU		

**Table 7-15 A20 Processor Interface Signatures (Cont'd)**

Signal Analyzer Setup:			
Signal	Polarity	Connection	
Clock		A20J200(3) "R $\overline{I}O\overline{S}$ "	
Start		A40J100(5)	
Stop		A40J100(4)	
+ 5 V Signature - H253			
Digital Filter Data Bus Latch			
U400(2)	0PFP	U402(2)	U78H
U400(3)	0P41	U402(3)	853F
U400(4)	4242	U402(4)	FHU5
U400(5)	8U1F	U402(5)	U91F
U400(6)	3A27	U402(6)	4UPA
U400(7)	UH59	U402(7)	64A5
U400(8)	PU57	U402(8)	H111
U400(9)	71AF	U402(9)	P6CA

**[V] TRIGGER TIMING, [X] COUNTER CLOCK SELECT, [AA] PRN CAL SIGNAL GENERATOR**

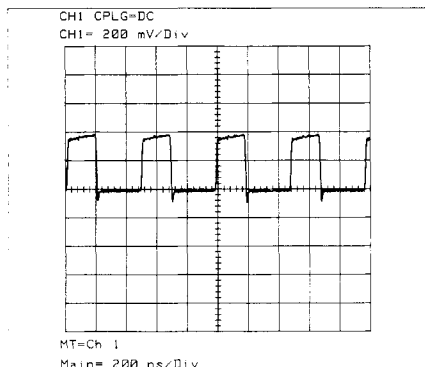
1. Set the -hp-3561A controls as follows:

```

PRESET
TRIGger SElect... TRIGGER
INTERNAL TRIGGER
INPUT..... CAL SIG ON
    
```

2. Check the waveforms as shown in Figure 7-13.

**Figure 7-13 A20 Counter Clock Waveforms**



```

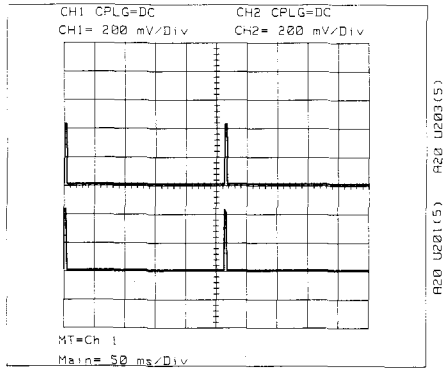
Probe: 10:1

Ch1: Connection- A20 U505(9) "U202 Clock"
A20 U300(3)
Coupling- dc
Ground- Center Graticule

Trigger: Internal- Ch1
Slope- Positive

Bandwidth Limit: OFF
    
```





Probe: 10:1

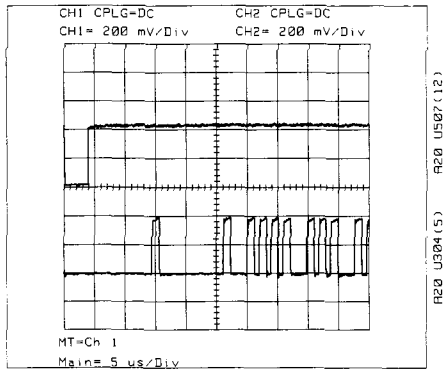
Ch1: Connection- A20 U203(5) "ITRIG"  
Coupling- dc  
Ground- Center Graticule

Ch1: Connection- A20 U201(5) "ITRIG"  
Coupling- dc  
Ground- Second Graticule from Bottom

Trigger: Internal- Ch1  
Slope- Positive

Bandwidth Limit: OFF

Note: the period of these signals alternates between 280 mSec, and 460 mSec.



Probe: 10:1

Ch1: Connection- A20 U507(12) "CAL TRIG"  
Coupling- dc  
Ground- Center Graticule

Ch2: Connection- A20U304(5) "PRN CAL"  
Coupling- dc  
Ground- Second Graticule from Bottom

Trigger: Internal- Ch1  
Slope- Negative

Bandwidth Limit: ON

**[W] PHASE COUNTER CLOCK, [Y] TIMING AND CONTROL COUNTER, [Z] COUNTER DATA BUS LATCH, [DD] CAL SIGNAL SELECT, [EE] TRIGGER SELECT**

1. Set the -hp-3561A Controls as follows:

```
PRESET
MODE ..... TEST SELECT ..... DEFINE TEST NUM ..... 121 ENTER
START CONT TST
```

2. Check the waveforms as shown in Figure 7-14.
3. If all of the waveforms given in Figure 7-14 are correct, set the -hp-3561A controls as shown below to run Test 13. If Test 13 fails with one or more return codes, the failure is most likely in U202, U300, or U600.

```
PRESET
MODE ..... TEST SELECT ..... DEFINE TEST NUM ..... 13 ENTER
START SNGL TST
```

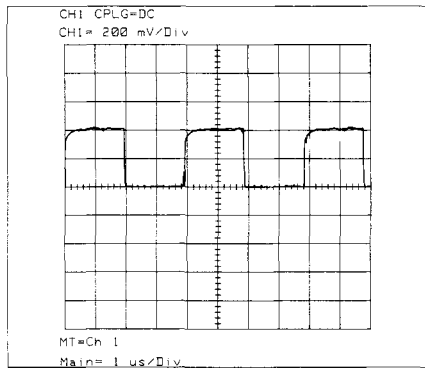
- If Test 13 passes with no return codes, set the -hp-3561A controls as follows:

```

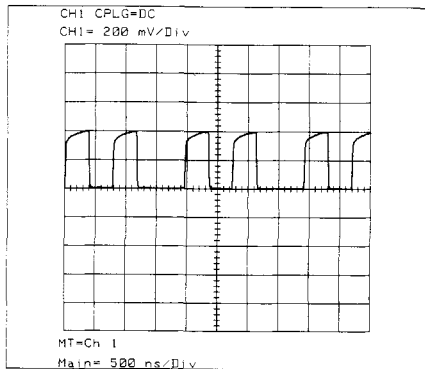
PRESET
TRIGger SElect... TRIGGER
                    INTERNAL TRIGGER
INPUT..... CAL SIG ON
    
```

- Check the waveforms given in Figure 7-15.

**Figure 7-14 Test 121 Counter Input Waveforms**



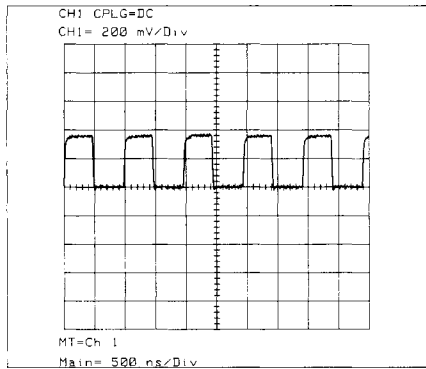
Probe: 10:1  
Ch1: Connection- A20 U300(6) "PHASE CLK"  
Coupling- dc  
Ground- Center Graticule  
Trigger: Internal- Ch1  
Slope- Positive  
Bandwidth Limit: ON



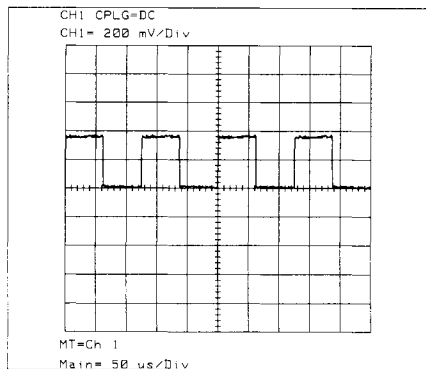
Probe: 10:1  
Ch1: Connection- A20 U300(11) "PHASE CLK"  
Coupling- dc  
Ground- Center Graticule  
Trigger: Internal- Ch1  
Slope- Positive  
Bandwidth Limit: ON

Note: The waveform at U202(31) will be the "or" of these two signals gated on and off by the ITRIG signal. The signal at U202(31) can be checked by triggering on either U300(6) or U300(11).

**Figure 7-15 A20 Counter Output Waveforms**



Probe: 10:1  
 Ch1: Connection- A20 TP701 "ESR\*4"  
 Coupling- dc  
 Ground- Center Graticule  
 Trigger: Internal- Ch1  
 Slope- Positive  
 Bandwidth Limit: ON



Probe: 10:1  
 Ch1: Connection- A20 U507(5) "CAL GEN"  
 Coupling- dc  
 Ground- Center Graticule  
 Trigger: Internal- Ch1  
 Slope- Positive  
 Bandwidth Limit: ON

**[B] CHANNEL R DMA COUNTER, [D] CHANNEL R ADDRESS BUS LATCH [I] RAM BUS INTERFACE, [K] DMA CHANNEL SELECT, [M] DIGITAL FILTER**

1. Set the -hp-3561A controls as follows:

```

PRESET
MODE ..... TEST SELECT..... DEFINE TEST NUM.....123 ENTER
START CONT TST
    
```

2. Check the waveforms given in Figure 7-16. These waveforms depend on the proper operation of the RAM bus interface, the DMA channel select, and the digital filter control IC (U4).
3. When the waveforms given in Figure 7-16 are correct, check the waveforms given in Figure 7-17 and the signatures given Table 7-16 to troubleshoot the channel R DMA counters.

- When the channel R DMA counter is operating correctly, Diagnostic Self Test #14 can be used to troubleshoot the real and imaginary digital filters. Set the -hp-3561A controls as follows:

```

PRESET
MODE ..... TEST SELECT.....DEFINE TEST NUM.....14 ENTER
START CONT TST
    
```

If no return codes are displayed, the digital filters are operational. If only even numbered return codes are displayed, the failure is in U4 or U401. If only odd numbered return codes are displayed the failure is in U4 or U1. If both odd and even numbered return codes are displayed, the failure could be in any one of the three digital filter ICs. To isolate the failure, either U1 or U401 can be removed. When U401 is removed, only even numbered errors should occur, and when U1 is removed, only odd errors should occur. U1 and U401 are completely interchangeable and can be swapped to see if the failure follows the digital filter. If the error does not follow the digital filter, the failure is in U4.

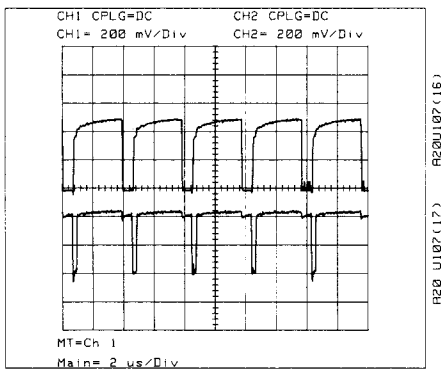
- To check the digital filter control IC (U4), set the -hp-3561A controls as follows:

```

PRESET
MODE ..... TEST SELECT.....DEFINE TEST NUM.....120 ENTER
START CONT TST
    
```

- Check the signatures given in Table 7-17.

**Figure 7-16 Test 123 RAM Bus Interface Waveforms**



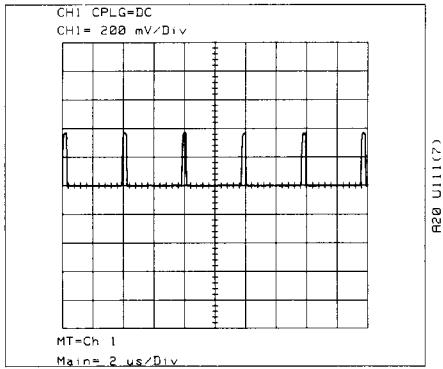
Probe: 10:1

Ch1: Connection- A20 U107(16) "DF2BR"  
 Coupling- dc  
 Ground- Center Graticule

Ch2: Connection- A20 U107(17) "DF2BG"  
 Coupling- dc  
 Ground- Second Graticule from Bottom

Trigger: Internal- Ch1  
 Slope- Negative

Bandwidth Limit: ON



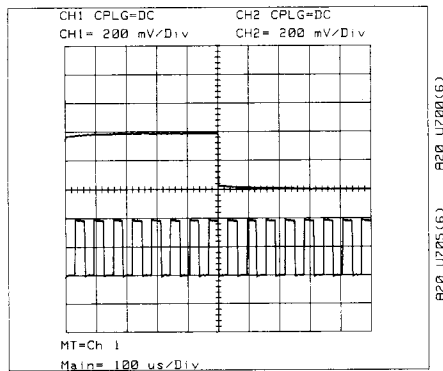
Probe: 10:1

Ch1: Connection- A20 U111(7) "BGR"  
Coupling- dc  
Ground- Center Graticule

Trigger: Internal- Ch1  
Slope- Positive

Bandwidth Limit: ON

**Figure 7-17 Test 123 Channel R DMA Counter Waveforms**



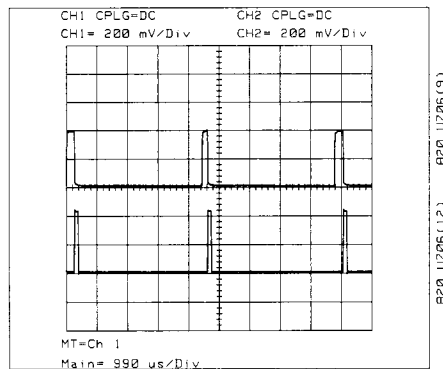
Probe: 10:1

Ch1: Connection- A20 U700(6)  
Coupling- dc  
Ground- Center Graticule

Ch2: Connection- A20 U705(6)  
Coupling- dc  
Ground- Second Graticule from Bottom

Trigger: Internal- Ch1  
Slope- Positive

Bandwidth Limit: ON



Probe: 10:1




Ch1: Connection- A20 U706(9) "DONER"  
Coupling- dc  
Ground- Center Graticule

Ch2: Connection- A20 U706(12) "ER"  
Coupling- dc  
Ground- Center Graticule




Trigger: Internal- Ch1  
Slope- Positive

Bandwidth Limit: ON

**Table 7-16 Test 123 Channel R Address Bus Latch Signatures**

<b>Signature Analyzer Setup</b>		
<b>Signal</b>	<b>Polarity</b>	<b>Connection</b>
Clock		A20U703(12) "BGR"
Start		A20U706(9) "DONER"
Stop		A20U706(9) "DONER"
+ 5 V Signature - 472A		
<b>Channel R Address Bus Latch</b>		
U603(2)	3H19	
U603(5)	14U7	
U603(6)	0431	
U603(9)	PPA9	
U603(12)	P30H	
U603(15)	8084	
U603(16)	1H4H	
U603(19)	6886	
U607(2)	94A3	
U607(5)	22FC	

**Table 7-17 Test 120 Digital Filter Signatures**

<b>Signature Analyzer Setup</b>		
<b>Signal</b>	<b>Polarity</b>	<b>Connection</b>
Clock		A20J100(3) "DFCLKφ1"
Start		A20J100(4) "CLR"
Stop		A20J100(5) "DSASTOP"
<p>Note: The stop and start connections are reversed from the labels printed on the PC board.</p> <p>+ 5 V Signature - 695A</p>		
<b>Digital Filter Interface Signals</b>		
U4(3)	03U9	
U4(19)	38HU	
U4(20)	H914	
U4(21)	54P2	
U4(36)	0 volts	
U4(49)	2208	
U4(50)	8UP9	
U4(51)	8UP9	
U4(52)	2208	
U4(59)	25P6	
U4(60)	U614	
U4(61)	F545	
U4(62)	U9AA	
U4(63)	H330	

**[C] CHANNEL G DMA COUNTER, [E] CHANNEL G ADDRESS BUS LATCH, [L] CHANNEL G COUNTER PRESET**

1. Set the -hp-3561A controls as follows:

```

PRESET
MODE ..... TEST SELECT.....DEFINE TEST NUM.....122 ENTER
                                START CONT TST
    
```

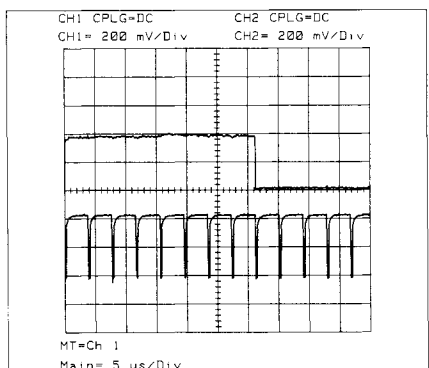
2. Check the waveforms given in Figure 7-18.
3. If all of the waveforms in Figure 7-18 are correct, check all of the signatures in Table 7-18.

- Set the -hp-3561A controls as follows:

PRESET  
 TRIGger SElect... TRIGGER  
 INTERNAL TRIGGER

- Check the waveform given in Figure 7-19.

**Figure 7-18 Test 122 Channel G DMA Counter Waveforms**



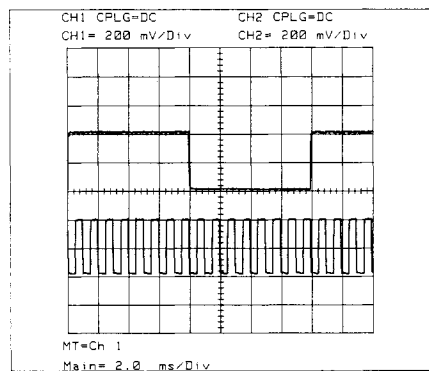
Probe: 10:1

Ch1: Connection- A20 U700(8) "G3"  
 Coupling- dc  
 Ground- Center Graticule

Ch2: Connection- A20 U703(8) "BGG"  
 Coupling- dc  
 Ground- Second Graticule from Bottom

Trigger: Internal- Ch1  
 Slope- Positive

Bandwidth Limit: OFF



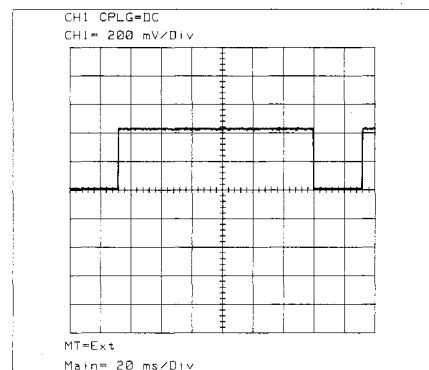
Probe: 10:1

Ch1: Connection- A20 U706(6) "GB"  
 Coupling- dc  
 Ground- Center Graticule

Ch2: Connection- A20 U705(8) "G7"  
 Coupling- dc  
 Ground- Second Graticule from Bottom

Trigger: Internal- Ch1  
 Slope- Positive

Bandwidth Limit: OFF



Probe: 10:1

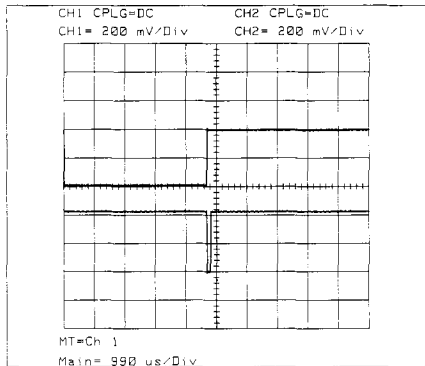
Ch1: Connection- A20 U508(11) "GCNTF"  
 Coupling- dc  
 Ground- Center Graticule

Trigger: External- U700(12) "EG"  
 Slope- Positive

Bandwidth Limit: OFF



**Figure 7-19 "DONEG" Waveforms**



Probe: 10:1




Ch1: Connection- A20 U106(1)  
Coupling- dc  
Ground- Center Graticule

Ch2: Connection- A20 TP703 "DONEG"  
Coupling- dc  
Ground- Second Graticule from Bottom

Trigger: Internal- Ch1  
Slope- Negative

Bandwidth Limit: ON

**Table 7-18 Test 122 Channel G Address Bus Latch Signatures**

Signature Analyzer Setup			
Signal	Polarity	Connection	
Clock		A20U703(8) " $\overline{\text{BGG}}$ "	
Start		A20U508(11) "GCNTF"	
Stop		A20U508(11) "GCNTF"	
+ 5 V Signature - 755U			
Channel G Address Bus Latch			
U602(2)	H335	U606(2)	7707
U602(5)	C113	U606(5)	577A
U602(6)	7050	U606(6)	HH86
U602(9)	0772	U606(9)	89F1
U602(12)	A3C1	U606(12)	755U
U602(15)	7211	U606(15)	1180
U602(16)	AA08	U606(16)	PCF3
U602(19)	C4C3	U606(19)	AC99

**[Q] DATA REQ/SYNC2 GENERATOR, [T] CONVERT SIGNAL SELECT [P] CONVERT SIGNAL TIMING**

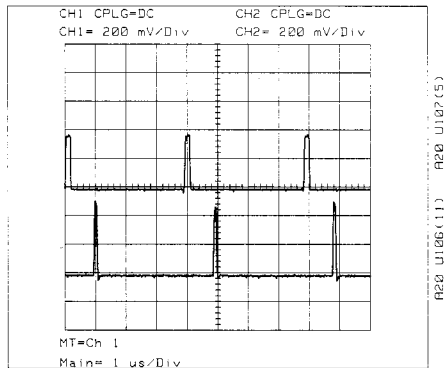
1. Set the -hp-3561A controls as follows:

```

PRESET
MODE ..... TEST SELECT .....DEFINE TEST NUM .....122 ENTER
START CONT TST
    
```

2. Check the waveforms given in Figure 7-20.

**Figure 7-20 Convert/Sync2 Waveforms In Test 122**



Probe: 10:1

Ch1: Connection- A20 U107(5) "CONVERT"  
Coupling- dc  
Ground- Center Graticule

Ch2: Connection- A20 U106(11) "SYNC2"  
Coupling- dc  
Ground- Second Graticule from Bottom

Trigger: Internal- Ch1  
Slope- Positive

Bandwidth Limit: ON

**Table 7-19 A20 Assembly Signal Connections**

**INPUTS**

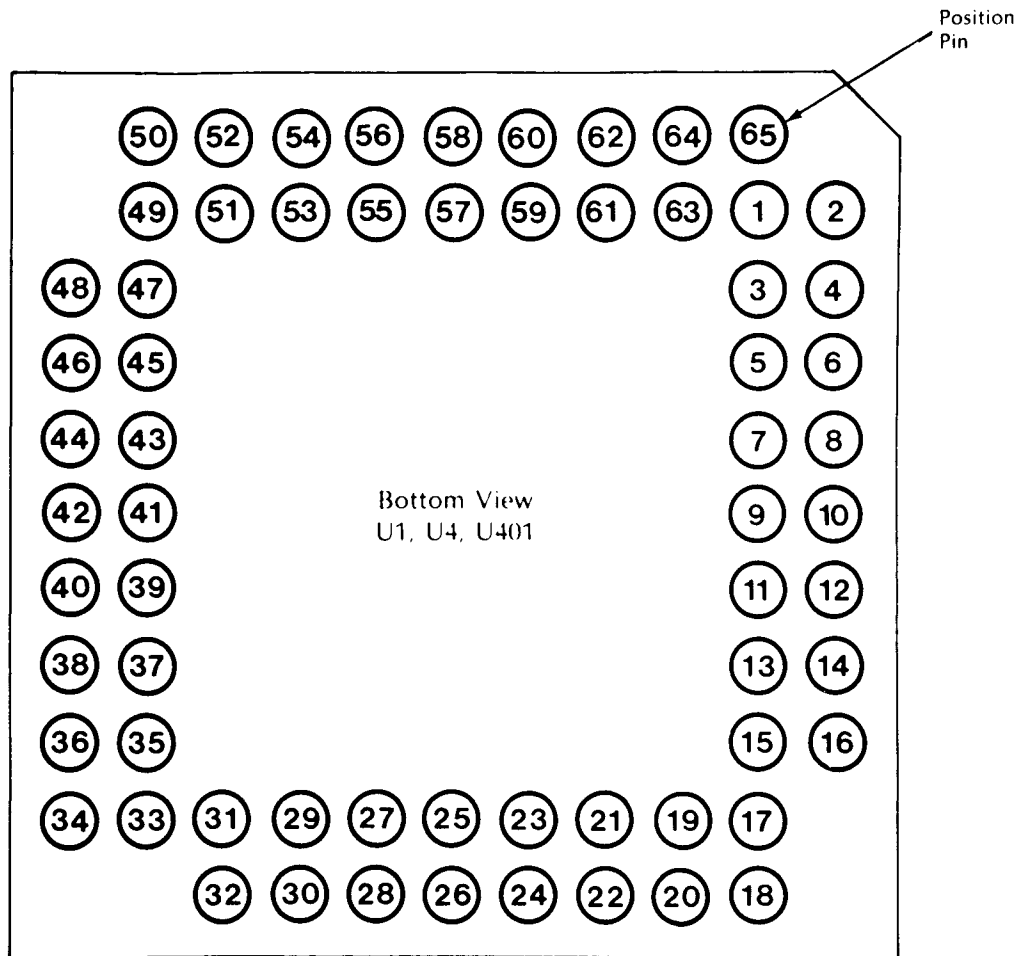
Signal Name	Functional Block	Connector Origin Number	Assembly
A/D DATA	U	P22(A2)	A15
COSINE	U	P21(A19)	A50
DF1BG	I	P22(A11)	A30
DF2BG	I	P22(A10)	A30
DF3BG	I	P22(A9)	A30
EXT SAMP	T	P22(A7)	A82
FEISO	BB	P21(A23)	S2 (front panel)
FETRIG	EE	P22(B5)	A15
RBR/W	F	P21(A10)	A30
RESET	H	P21(A21)	A40
RIOS	F	P21(B10)	A30
-SINE	U	P21(B19)	A50
SSTAT	O	P22(B4)	A15
1/3TRIG	EE	P22(B7)	A50
20.48 MHz	FF	P21(B24)	A40

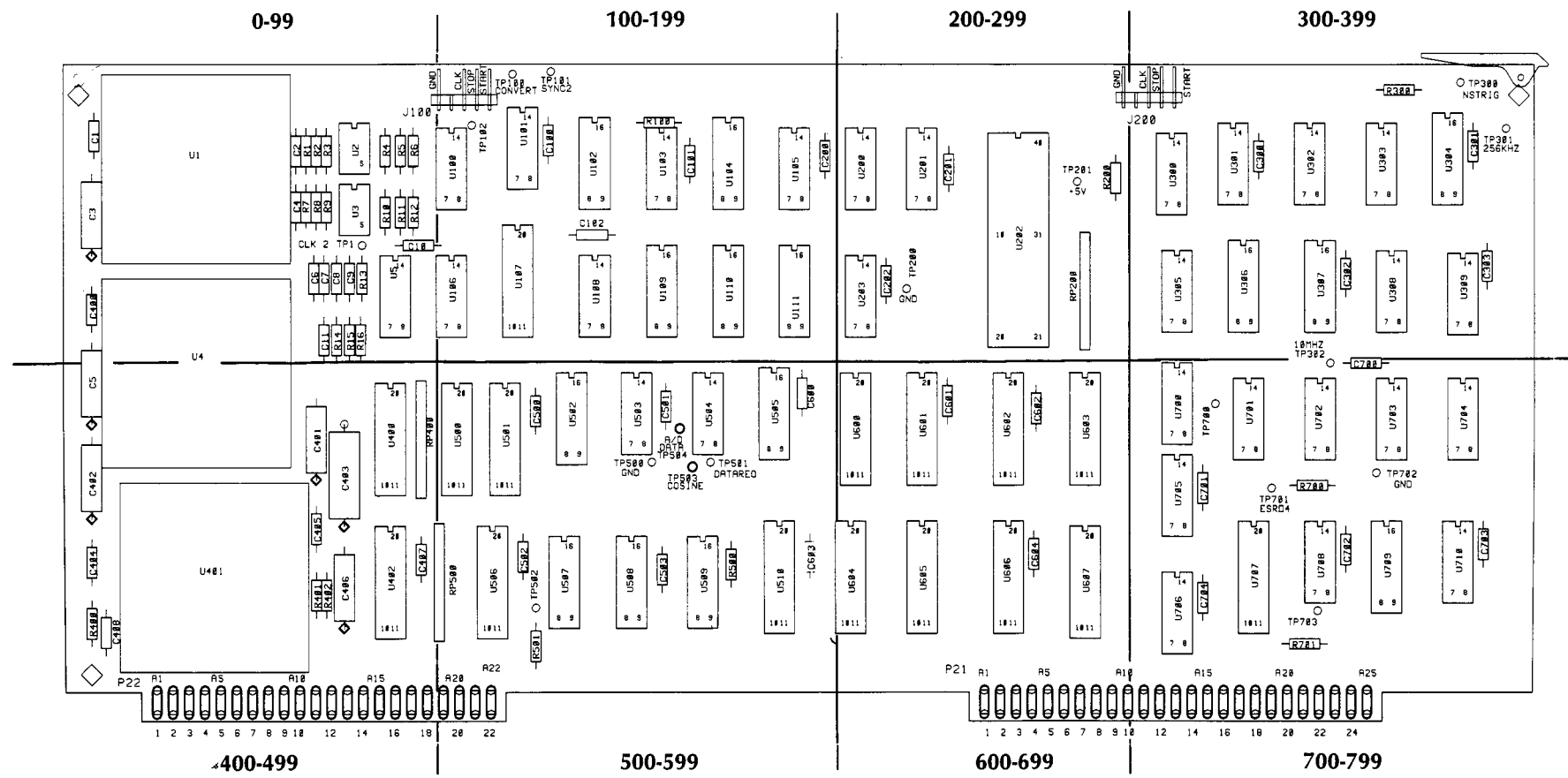
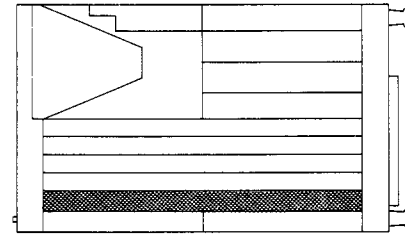
## OUTPUTS

Signal Name	Functional Block	Connector Number	Destination Assemblies
CONVERT	P	P22(B2)	A15
DATA REQ	Q	P22(B3)	A15
DMAI	Y	P21(B16)	A40
DF1BR	I	P22(B11)	A30
DF2BR	I	P22(B10)	A30
DF3BR	I	P22(B9)	A30
ESR*4	Y	P21(A23)	A50
FE CAL	DD	P21(B12)	A10
FECLK	S	P21(B11)	A10
FEDATA	S	P21(A11)	A10
FELATCH	S	P21(A12)	A10
SYNC2	Q	P21(B18)	A50
ZPHTRIG	V	P21(A17)	A50
256 KHz	GG	P21(B23)	A70
10.24 MHz	FF	P21(A24)	A15, A50

## I/O SIGNALS

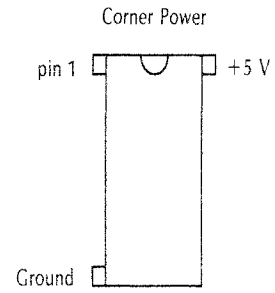
Signal Name	Functional Block	Connector Number	Destination Assemblies
RAM Address Bus RAB0 - RABF	A	P21(A2 - A9) P21(B2 - B9)	A30, A40
RAM Data Bus RDB0 - RDBF	R	P22(A12 - A19) P22(B12 - B19)	A30





A20 Assembly

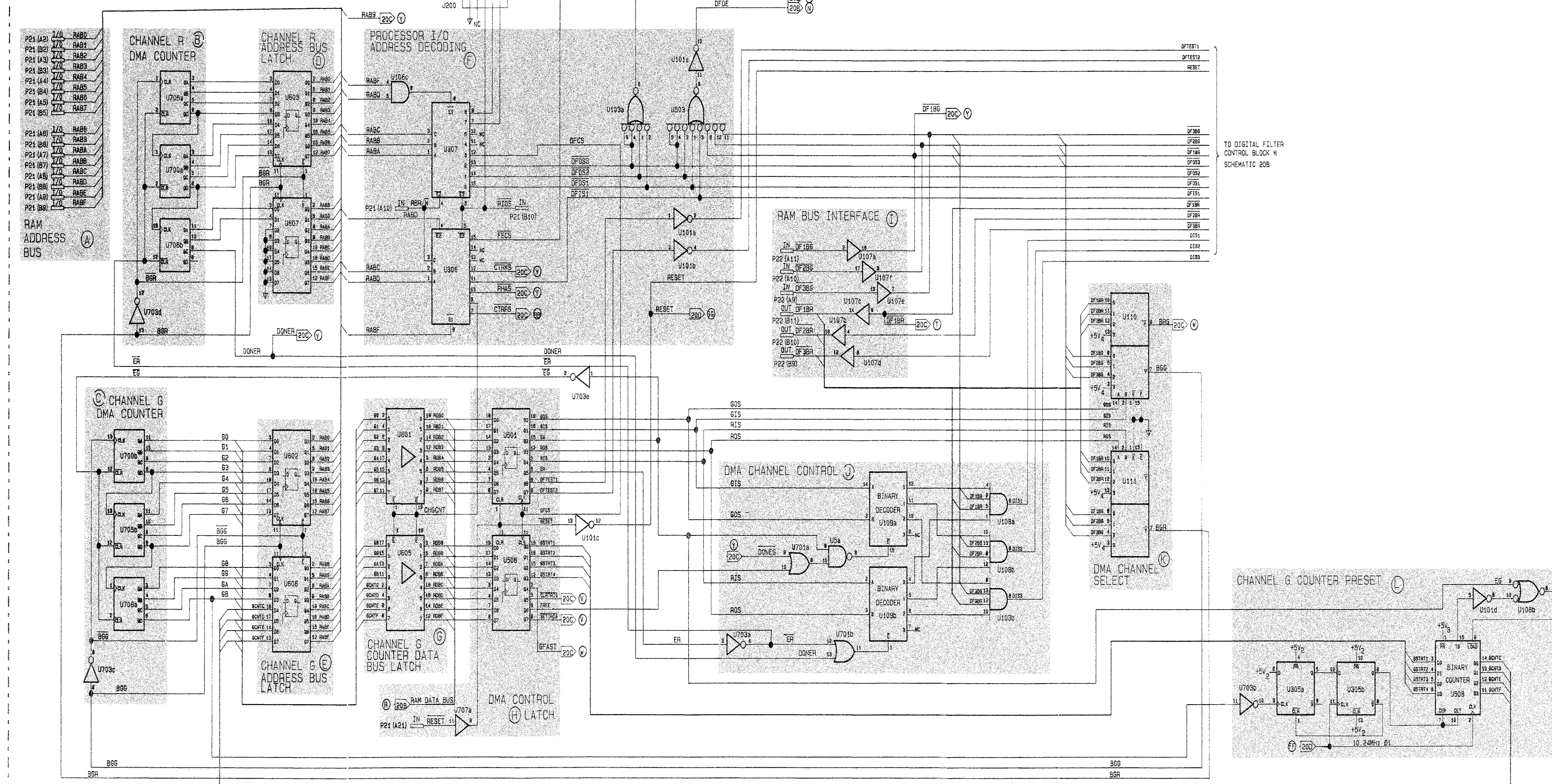
All integrated circuits are corner powered except those shown in the table below. Corner powered ICs have ground connected to the lower left pin, and +5 V connected to the upper right pin regardless of the total pin count. (eg, for a 16 pin DIP, ground is connected to pin 8 and +5 V is connected to pin 16)



	+8V	+5V	-2V	GND
U1	7,9 40,42	8,41	1	17,32 49,64
U2	7			3
U3	7			3
U4	2,48	22	1	58
U202	7,9	1		21
U401	7,9 40,42	8,41	1	17,32 49,64

DIGITAL FILTER ASSEMBLY

03561-66520  
REV B



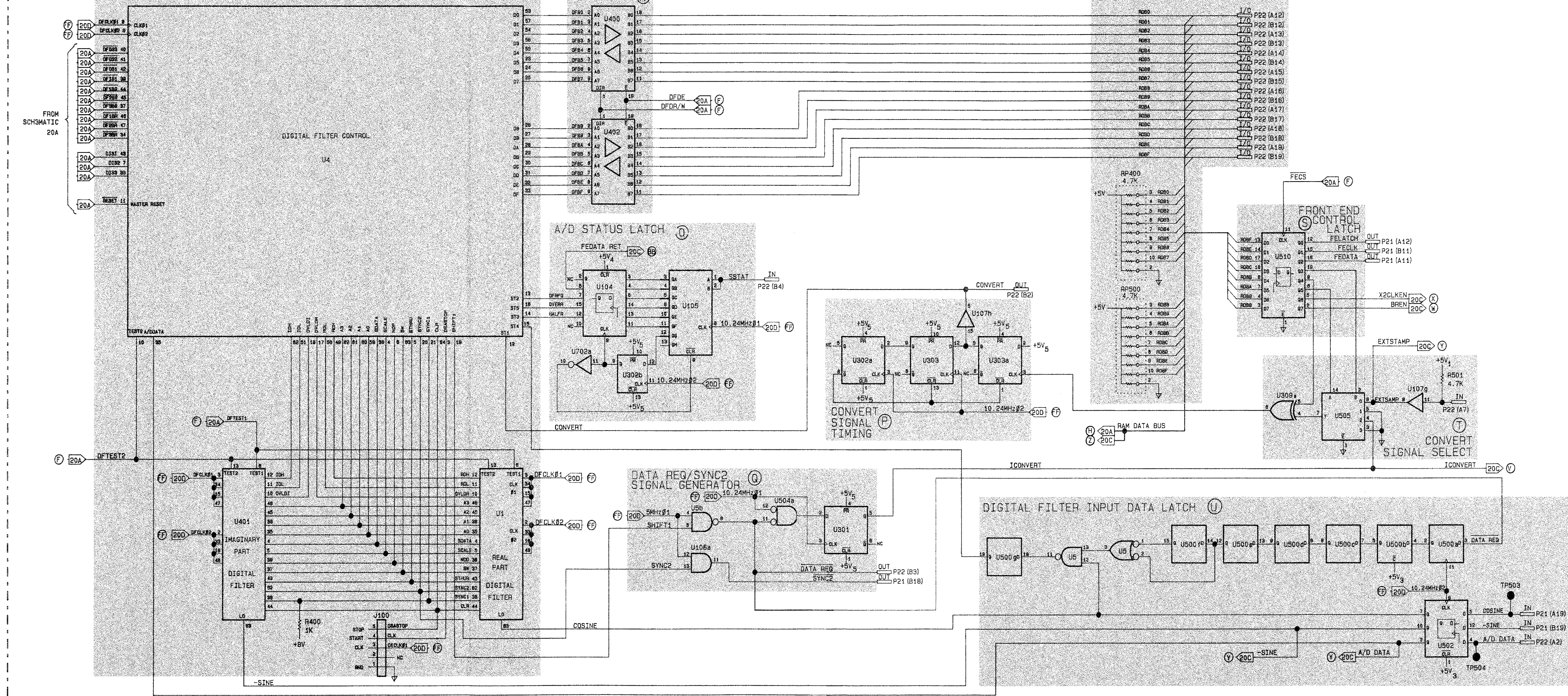
TO DIGITAL FILTER CONTROL BLOCK N SCHEMATIC 20B



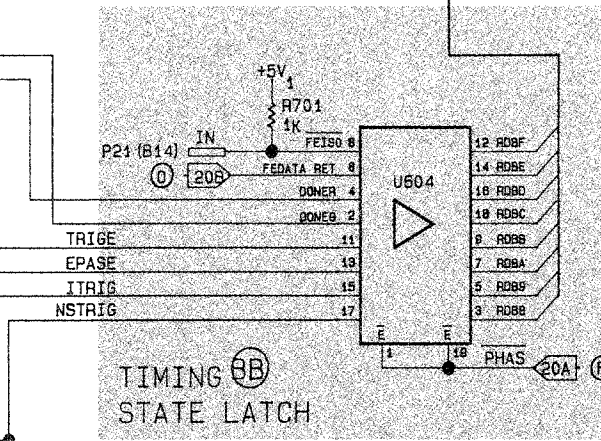
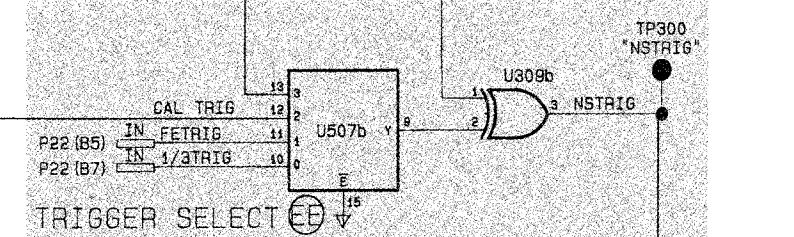
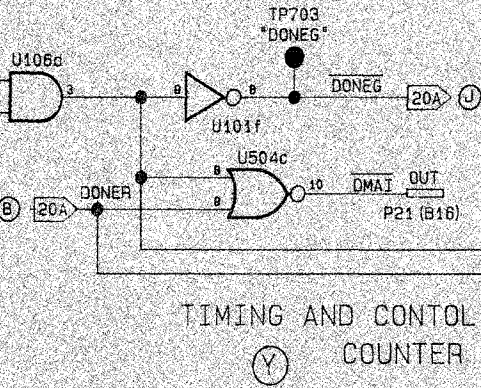
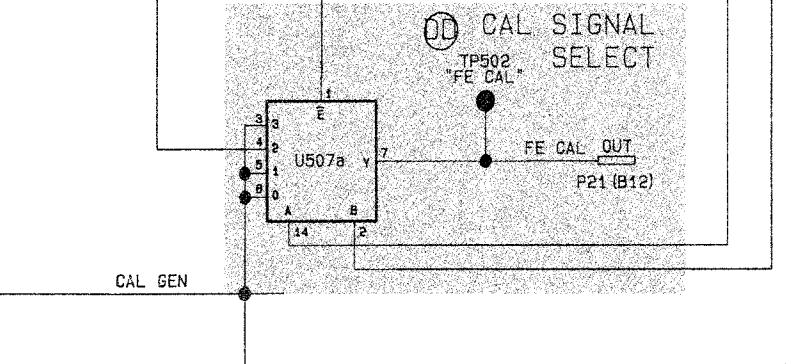
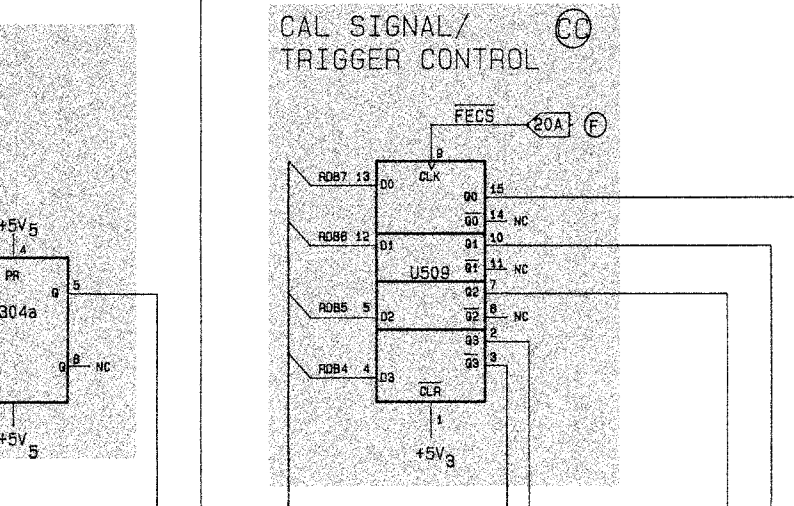
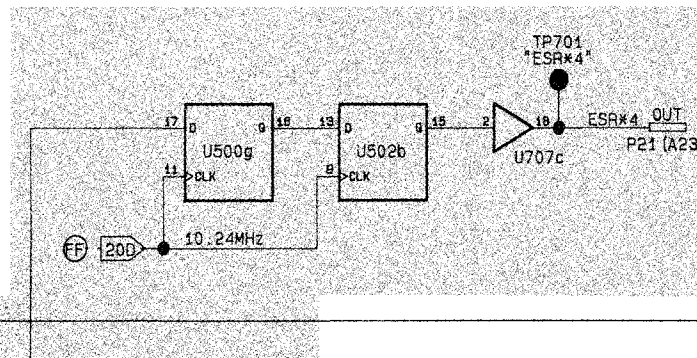
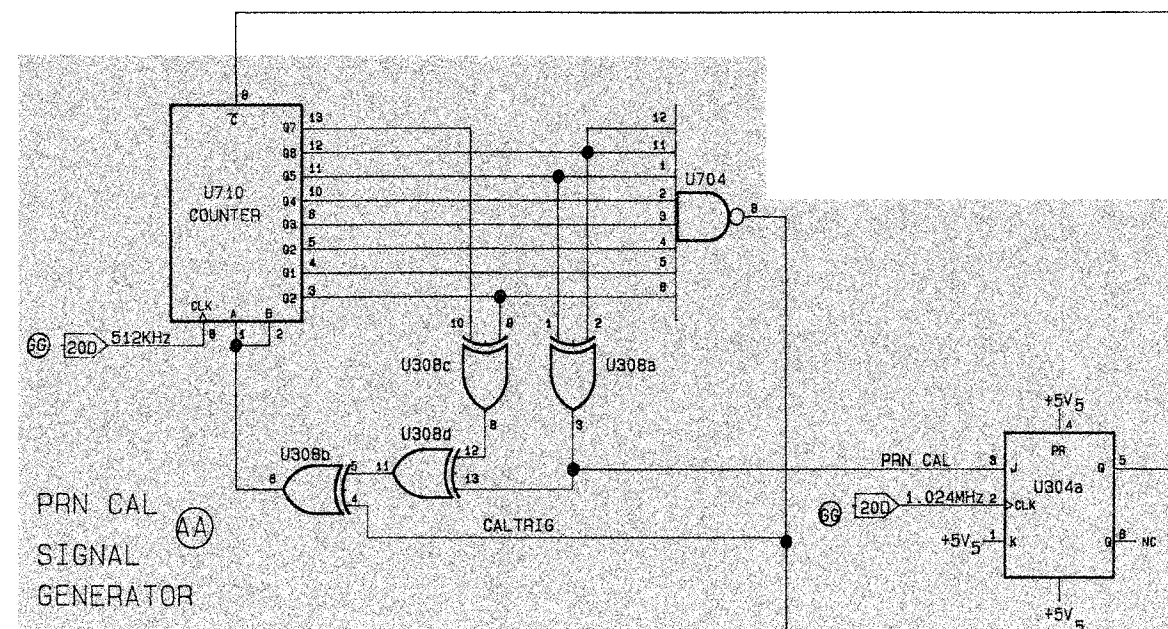
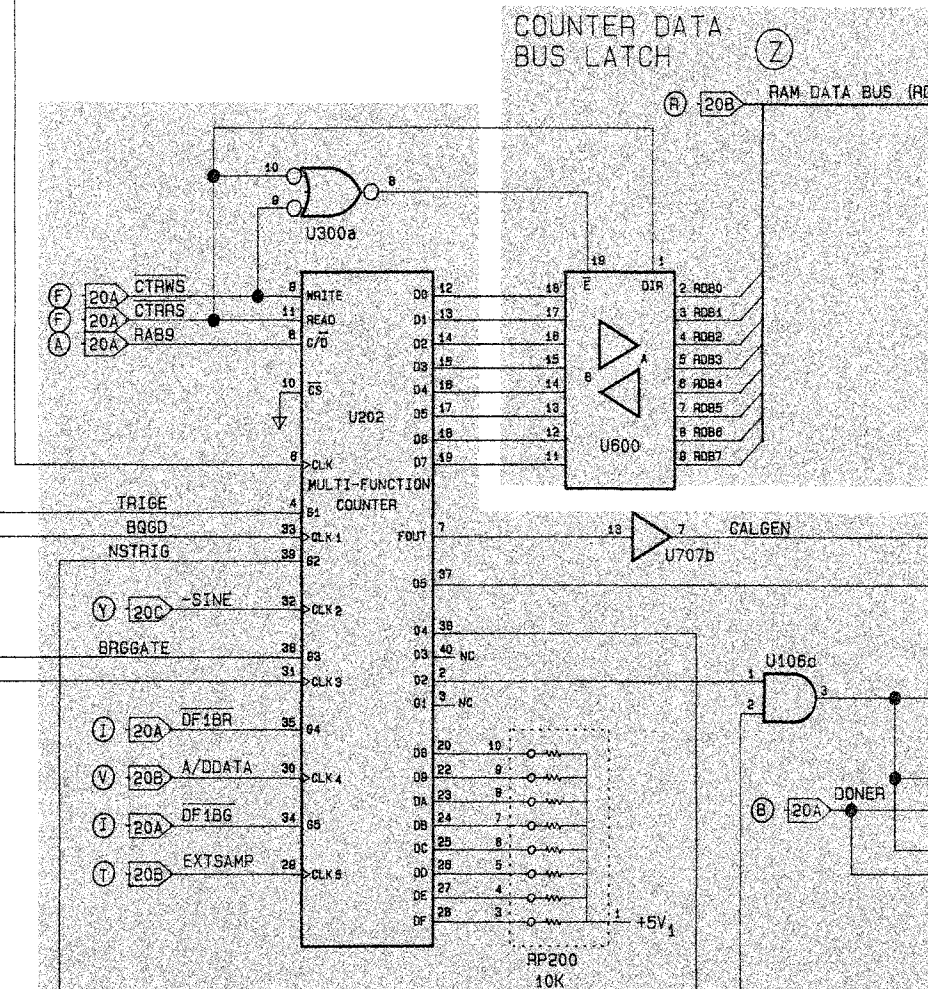
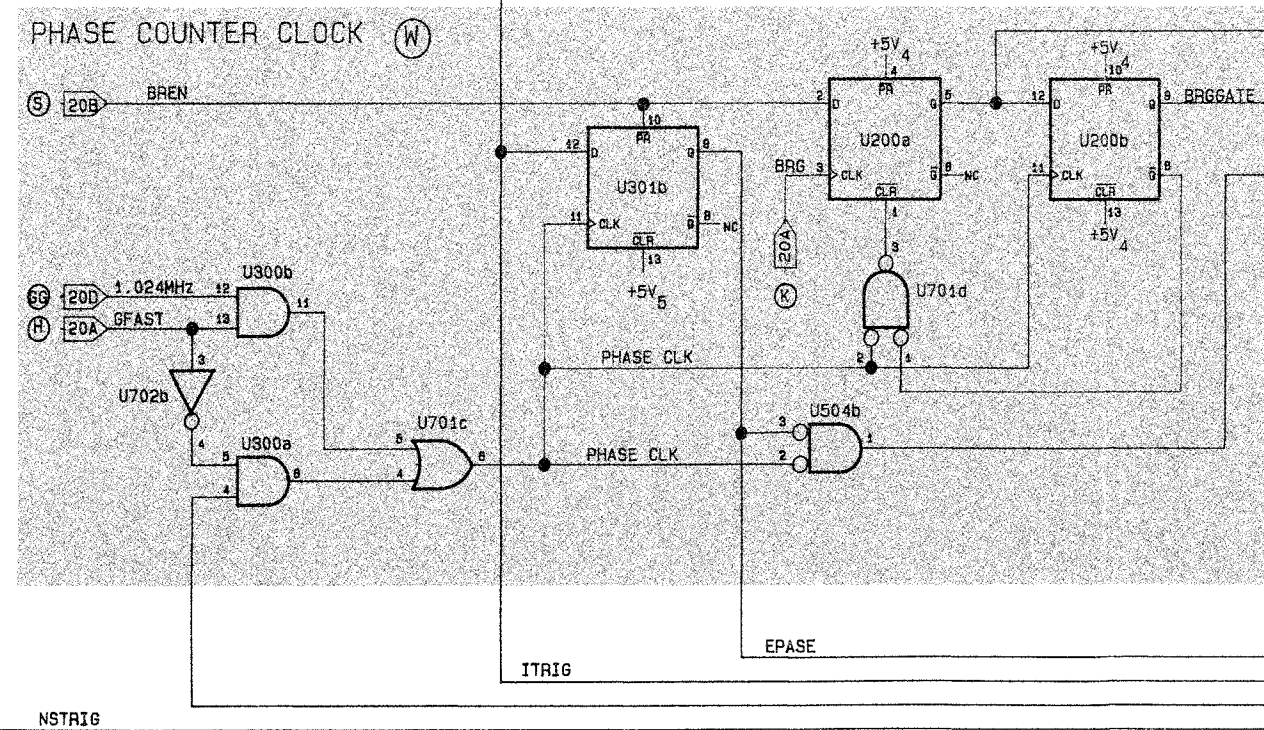
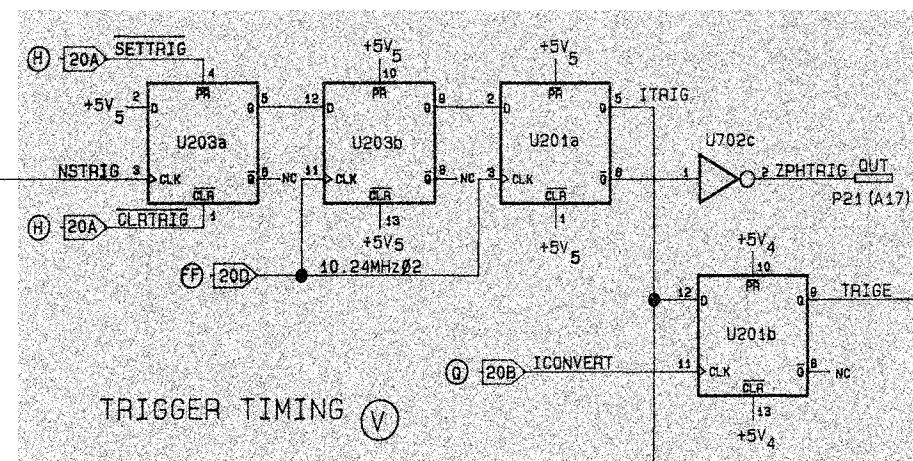
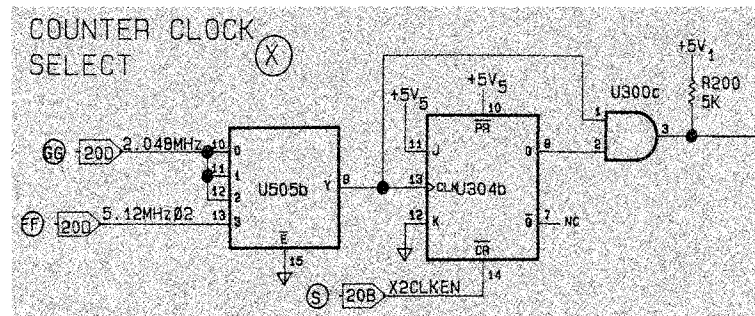
DIGITAL FILTER (M)

DIGITAL FILTER DATA BUS LATCH (N)

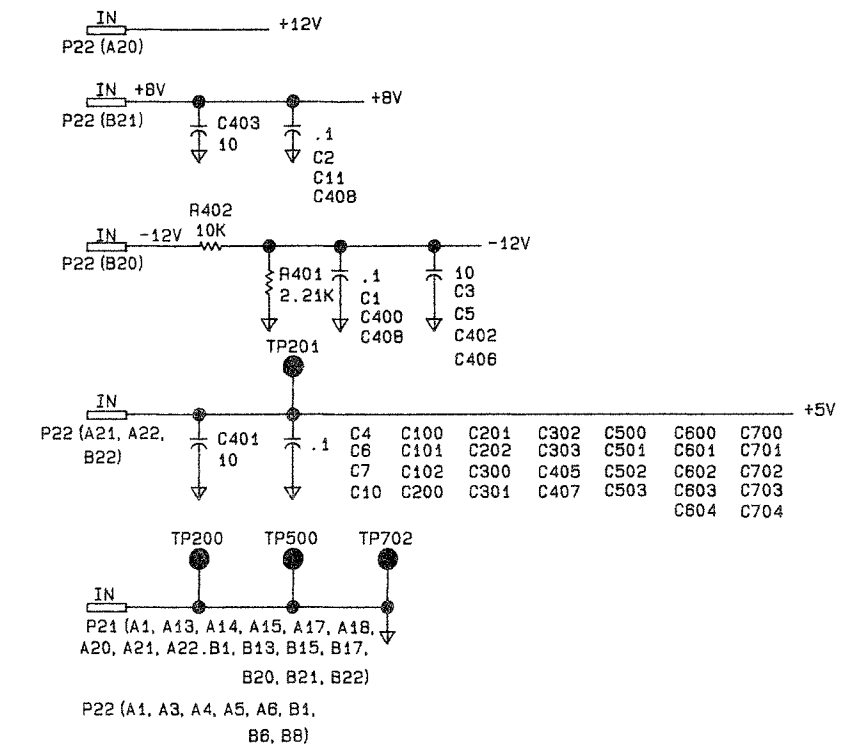
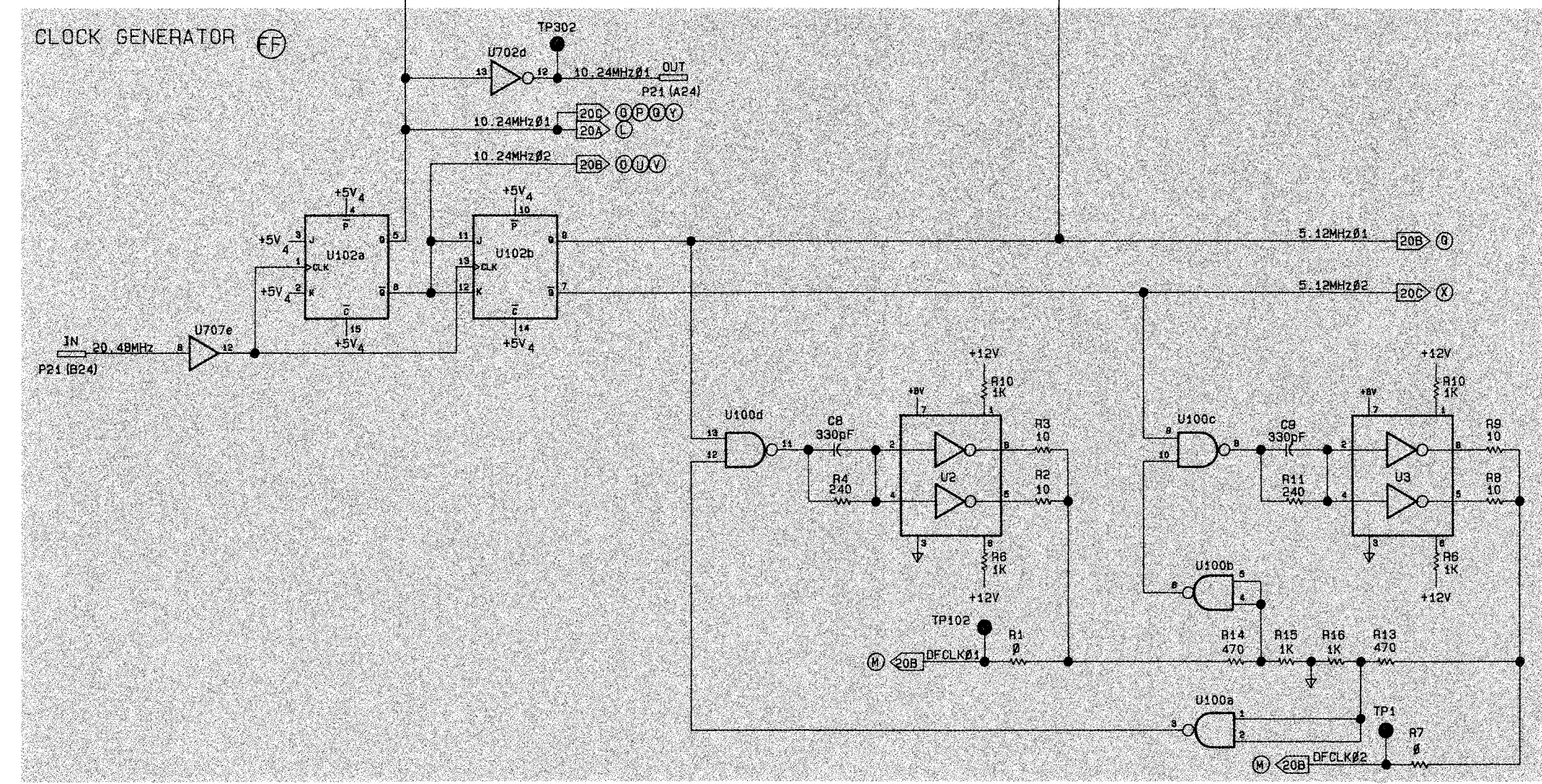
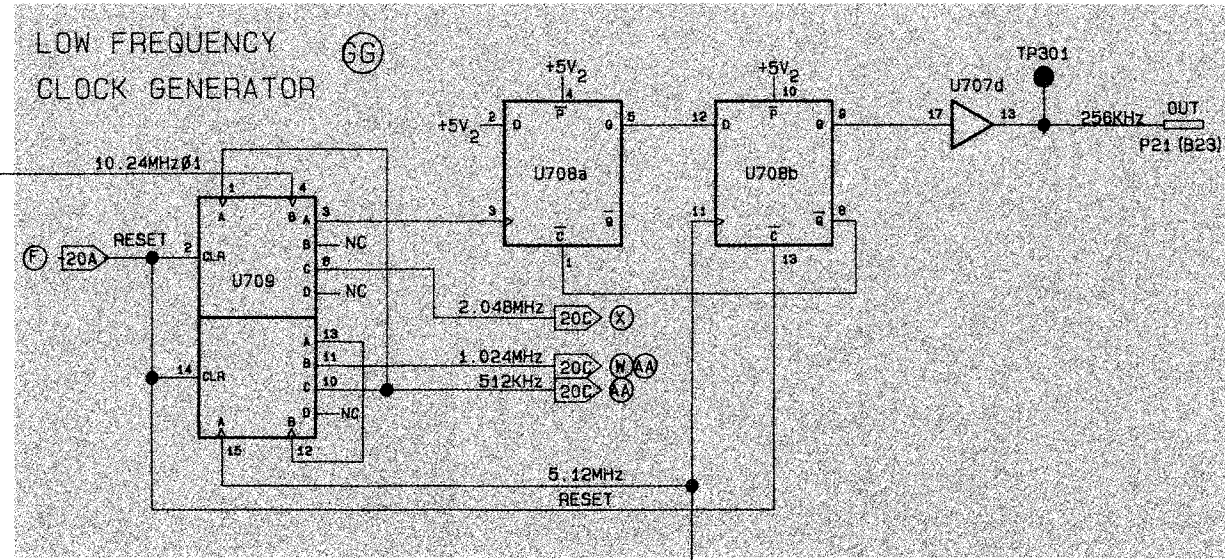
RAM DATA BUS (R)











## 7-13 A30 FFT/RAM ASSEMBLY

### 7-14 FFT/RAM Circuit Description

#### GENERAL

The A30 Assembly contains the instrument RAM and the FFT processor. The instrument RAM is accessed for data storage by three circuits: the central processor, the FFT processor, and the digital filter. Access to the RAM bus is regulated by the RAM bus arbitrator, which prevent these three circuits from interfering with one another.

The FFT processor is an asynchronous microprocessor dedicated to performing the Fast Fourier Transform. An FFT is initialized by the main processor through the  $\overline{\text{FFT}} \overline{\text{RESET}}$  signal.

#### RAM BUS STRUCTURE

The -hp-3561A has a two bus structure for transferring data between circuits. The processor bus is controlled by the central microprocessor on the A40 Assembly and the RAM bus is controlled by the RAM bus arbitrator on the A30 Assembly. The RAM bus consists of a 16 bit data bus and a 16 bit address bus. To access the RAM bus, a circuit must issue a bus request signal to the RAM bus arbitrator. The RAM bus arbitrator then issues a bus grant to the highest priority bus request. In addition to direct RAM access, the RAM bus is used by the central processor to transfer I/O data to the A20 and A30 Assemblies.

#### [D] MAIN RAM

The A30 Assembly contains sixteen 64k by 1 bit RAMs. The RAM is addressed in a two step process. First, an 8 bit row address is placed on the memory address bus, which is latched by the RAM on the rising edge of  $\overline{\text{RAS}}$ . Second, an 8 bit column address is placed on the memory address bus, which is latched by the RAM on the rising edge of  $\overline{\text{CAS}}$ . The RAM either reads data from, or writes data to the the memory data bus on the rising edge of  $\overline{\text{CAS}}$ .

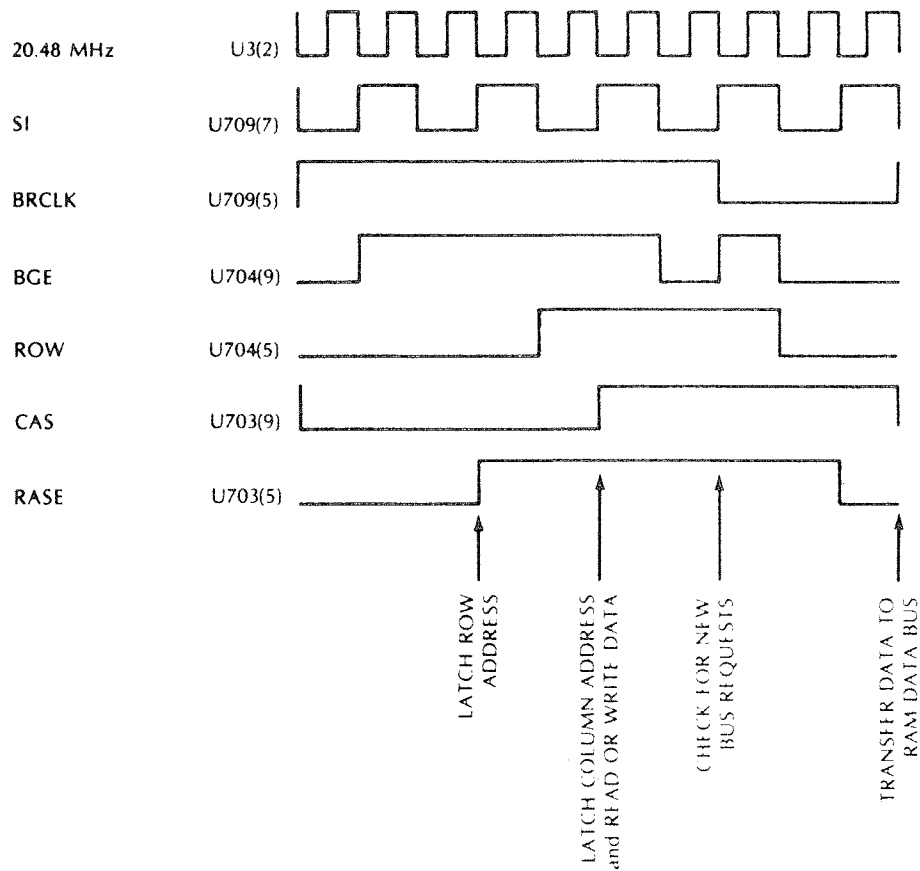
#### [B] RAM ADDRESS SELECTOR, [F] RAM COLUMN ADDRESS STROBE

When the ROW signal is low, the RAM address selector reads the row address from the lower 8 bits of the RAM address bus and when the ROW signal is high, the RAM address selector reads the column address from the upper 8 bits of the RAM address bus. The RAM column address strobe allows the processor to perform 8 bit or 16 bit operations by allowing access to just the lower 8 bits of RAM, just the upper 8 bits of RAM, or both.

**[E] RAM ACCESS STATE MACHINE**

This state machine generates all of the timing signals which control the RAM bus cycle. Figure 7-21 gives a timing diagram of the state machine outputs.

**Figure 7-21 RAM Access State Machine Timing**



**[I] RAM BUS ARBITRATOR**

The RAM bus arbitrator is a priority decoder which controls access to the RAM bus. When the RAM bus arbitrator receives a bus request signal, it compares the request against any other bus requests it has received. A bus grant signal is then issued to highest priority requester. The RAM bus arbitrator checks for new bus request signals once per RAM bus cycle on the rising edge of the BGE signal.

**[G] 100 kHz REFRESH CLOCK, [J] RAM REFRESH COUNTER**

The refresh clock issues a RAM bus request every ten micro seconds. If a bus grant is not received before the next ten micro second period, a higher priority bus request is issued. When a bus grant is received from the RAM bus arbitrator, the refresh counter addresses the memory location to be refreshed on the next RAM bus cycle.

**[K] RAM READ/WRITE GENERATOR**

This circuit determines what type of operation will occur on the next RAM bus cycle. When the  $\overline{\text{PRIOS}}$  signal is high, a read from or write to RAM operation occurs and when the  $\overline{\text{PRIOS}}$  signal is low, a processor I/O operation occurs.

**[O] FFT PROCESSOR**

When the FFT processor receives an  $\overline{\text{FFT RESET}}$  signal from the main processor, it begins to execute the instructions stored in the FFT ROM. The FFT processor reads 1024 time data points from the RAM, performs an FFT on the data, and then writes the results back into RAM. When the complete 1024 point FFT is complete, the FFT processor issues an interrupt ( $\overline{\text{FFTI}}$ ), which indicates to the central processor that the FFT is complete, and the results can be displayed on the CRT. The FFT processor runs on its own 20.00 MHz crystal oscillator.

**[U] FFT/RAM INTERFACE**

When the FFT processor wishes to access RAM, it issues a RAM bus request ( $\overline{\text{FFTBR}}$ ) through the FFT/RAM interface. On receipt of a RAM bus grant, the FFT/RAM interface clears the bus request and latches the RAM address onto the RAM address bus. The FFT processor then uses the FFT/RAM interface to transfer data to or from the RAM.

**Table 7-20 A30 Assembly Signal Descriptions**

<b>Signal</b>	<b>Description</b>
BRCLK	Bus Request CLock: Clocks the RAM bus request signals into the RAM bus arbitrator once per RAM bus cycle.
CASL	Column Address Strobe Lower 8 bits (bits 0-7): On the rising edge of this signal, the lower 8 bit RAMs latch the column address from the address bus and data from the memory data bus.
CASU	Column Address Strobe Upper 8 bits (bits 8-F): On the rising edge of this signal, the upper 8 bit RAMs latch the column address from the address bus and data from the memory data bus.
DBE	Data Bus Enable: Enables data transfer between the RAM and the RAM data bus through the RAM data bus buffers.
DEN	Data input ENable: Enables Data to be input to the FFT processor from the RAM data bus.
DF1BC	Digital Filter Channel (1,2,3) Bus Grant: These signals go low give the digital filter access to the RAM bus for storing type one, two or three data.
DF2BC	
DF3BC	
DF1BR	Digital Filter Channel (1,2,3) Bus Request: Issued by the digital filter to request access to the RAM bus.
DF2BR	
DF3BR	
FAB0-FABB	FFT Address Bus (12 bit): Used by the FFT processor to address the FFT instruction ROM.
FDB0-FDBF	FFT Data Bus (16 bit): Transfers data from ROM to the FFT processor and transfers data between the FFT processor and RAM.
FFTBC	FFT Bus Grant: Grants the FFT processor access to the RAM bus.
FFTBR	FFT Bus Request: Issued by the FFT processor to request access to the RAM bus. Highest priority request.
FFTCONS	FFT CONTROL Select: Clocks FFT control data into the FFT/Processor Interface Register.
FFTI	FFT Interrupt: Signals the central processor that the FFT processor has completed an FFT on a time record.
FFTINTCLR	FFT INTerrupt CLear: Issued by the processor to clear the FFT interrupt.
FFT RESET	FFT RESET: Issued by the central processor to reset the FFT processor and initialize an FFT on a new time record.
MEN	Memory ENable: Issued by the FFT processor to address the FFT ROM.
NODBE	NO Data Bus Enable: Inhibits a data bus enable when the processor is transferring I/O data over the RAM bus rather than directly accessing the RAM.
NOCAS	NO Column Address Strobe: Inhibits a column address strobe during RAM refresh.

**Table 7-20 A30 Assembly Signal Descriptions (Cont'd)**

<b>Signal</b>	<b>Description</b>
$\overline{\text{PBG}}$	Processor Bus Grant: This signal goes low to give the processor access to the RAM bus on the next RAM bus cycle.
$\overline{\text{PBLDS}}$	Processor Bus Lower Data Strobe: Low when the processor is addressing the the lower 8 bits of RAM.
$\overline{\text{PBR}}$	Processor Bus Request: Issued by the processor to request access to the RAM bus.
$\overline{\text{PRAMRE}}$	Processor RAM REad: Low to enable data from the RAM data bus onto the processor data bus in a RAM read or I/O port read operation.
$\overline{\text{PRIOS}}$	Processor Ram I/O Select: High when the processor is accessing RAM, low when the processor is accessing an I/O port through the RAM bus.
$\overline{\text{PBU DS}}$	Processor Bus Upper Data Strobe: Low when the processor is addressing the upper 8 bits of RAM.
$\overline{\text{RAS}}$	Row Address Strobe: On the rising edge of $\overline{\text{RAS}}$ the RAM latches the row address.
$\overline{\text{REFEN}}$	REFresh ENable: Gives the refresh counter access to the RAM bus. The refresh counter address increments by one each time a $\overline{\text{REFEN}}$ is received.
$\overline{\text{REFSEL}}$	REFresh SElect: Low to disable the refresh request issued by the 100 kHz refresh clock.
$\overline{\text{ROW}}$	ROW: High to indicate that the column address is on the memory address bus and low to indicate that the row address is on the memory address bus.
$\overline{\text{WE}}$	Write Enable: Issued by the FFT processor when it writes to RAM.

## 6-15 Troubleshooting the A30 Assembly

### GENERAL

Failures in the RAM will generally be flagged by the power on test. Failures in the FFT will generally result in no data or bad data being displayed on the CRT also causing the power on test to fail. Because the FFT processor has the highest priority access to the RAM, some FFT failures will prevent the central processor from accessing RAM, and thus appear as a RAM failure.

Troubleshoot the circuits on the A30 Assembly in the order given in Table 7-21. In this table, level one circuits must be operational before level two circuits can be tested, which must be operational before level three circuits can be tested and so on.

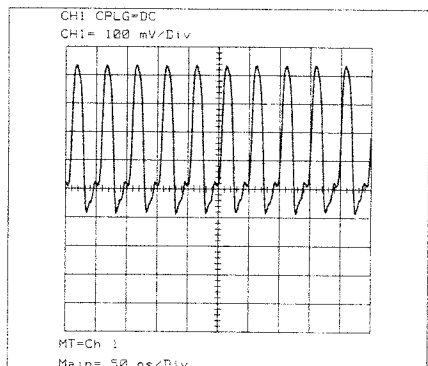
**Table 7-21 A30 Circuit Troubleshooting Order**

Level	Functional Blocks
1	Ram Access State Machine: E, C 100 kHz Refresh Clock: G
2	RAM Column Address Strobe: F RAM Bus Arbitrator: H, I, K
3	RAM Refresh Counter: J
4	Processor Interface: L, R, U
5	RAM: D RAM Address Bus: B RAM Data Bus: A
6	FFT Processor: M, N, O, P, S, T, V

**[E] RAM ACCESS STATE MACHINE**

Due to the feedback in the RAM access state machine, a failure on one signal will cause all of the signals to be incorrect. The correct output waveforms are given in Figure 7-22. Check the 20.48 MHz clock and the  $\overline{SI}$  signal first.  $\overline{SI}$  depends only on the clock. If these signals are correct, check the remaining signals. If these remaining signals are incorrect, replace U709, U704, U703, U702, U311, and U305 one at a time until the waveforms are correct. Recheck the waveforms after each IC is replaced.

**Figure 7-22 RAM State Machine Waveforms**

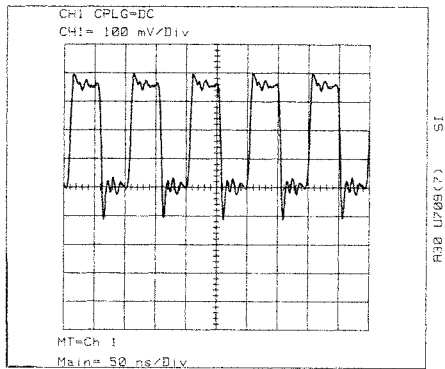


Probe: 10:1

Ch1: Connection- A30U709(1) "20.48 MHz"  
Coupling- dc  
Ground- Center Graticule

Trigger: Internal- Ch1  
Slope- Positive

Bandwidth Limit: OFF

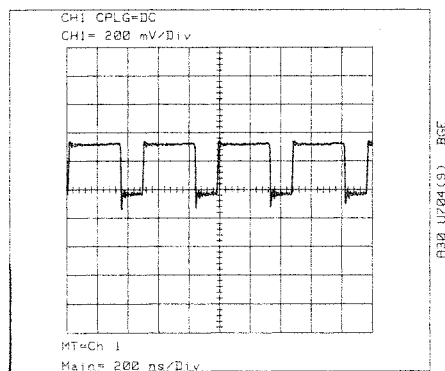


Probe: 10:1

Ch1: Connection- A30U709(7) "SI"  
Coupling- dc  
Ground- Center Graticule

Trigger: Internal- Ch1  
Slope- Positive

Bandwidth Limit: OFF

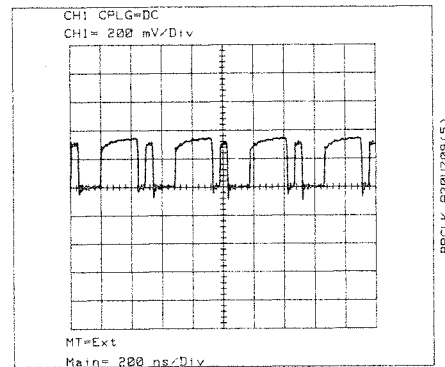


Probe: 10:1

Ch1: Connection- A30U704(9) "BGE"  
Coupling- dc  
Ground- Center Graticule

Trigger: Internal- Ch1  
Slope- Positive

Bandwidth Limit: OFF

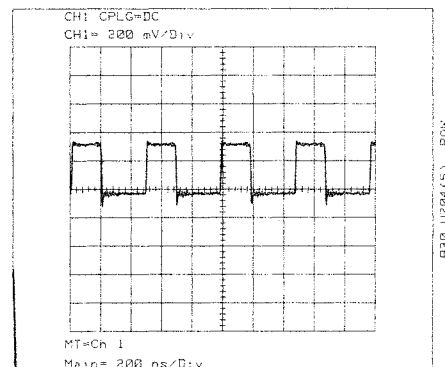


Probe: 10:1 and Trigger

Ch1: Connection- A30U709(5) "BRCLK"  
Coupling- dc  
Ground- Center Graticule

Trigger- External: A30U704(9) "BGE"  
Slope- Negative

Bandwidth Limit: OFF



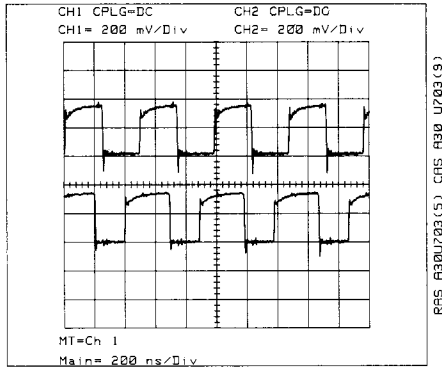
Probe: 10:1

Ch1: Connection- A30U704(5) "ROW"  
Coupling- dc  
Ground- Center Graticule

Trigger: Internal- Ch1  
Slope- Positive

Bandwidth Limit: OFF





Probe: 10:1

Ch1: Connection- A30U703(9) "CAS"  
Coupling- dc  
Ground- Center Graticule

Ch2: Connection- A30U703(5) "RAS"  
Coupling- dc  
Ground- Center Graticule

Trigger: Internal- Ch1  
Slope- Positive

Bandwidth Limit: OFF

#### [H] RAM BUS ARBITRATOR, [I] BUS GRANT TIMING, [G] 100 kHz REFRESH CLOCK

1. Turn the -hp-3561A LINE power switch OFF.
2. Remove the A20 Assembly and use a clip lead to short the the two pins of A30W100 together.
3. Move test jumper A40W1 to the test position.
4. Turn the -hp-3561A LINE power switch ON.
5. When the "BLT TEST ROUTINE" message is displayed, verify that U707(3, 4, 7, 8, 13) are all at a TTL high state. If these signals are all correct, check the waveforms given in Figure 7-23. These waveforms trace the Processor bus request signal and the refresh enable signal through the RAM bus arbitrator.

#### NOTE

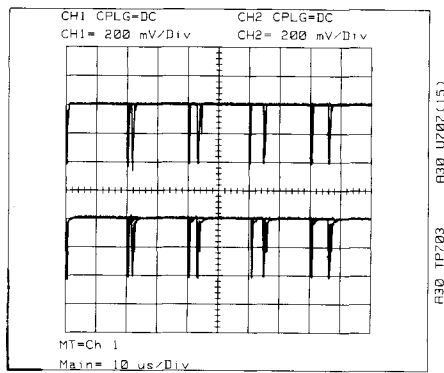
*The A60 Assembly may be removed during this test to disable the beeper. However, this also disables the display so the "BLT TEST ROUTINE" will not be displayed. The waveforms and signatures will be valid when the front panel LEDs begin to blink.*

6. Use a clip lead to short A30TP704 (DG3BR) to ground, simulating a constant digital filter bus request.
7. Check the signals listed in Table 7-22 and the waveforms given in Figure 7-24. While DF3BR is shorted to ground it is the highest priority bus request. The refresh enable signal and all bus grant signals except DF3BC should be inactive. This test may be repeated for DF2BG and DF1BG.
8. When all of the waveforms and signatures have been checked, move jumper A40W1 back to the run position, re-insert the A20 Assembly, and remove the short from A30W100.

**Table 7-22 RAM Bus Arbitrator Signals With DF3BR Grounded**

Signal	State
U707(2)	TTL High
U708(6)	Low
U708(7)	Low
U708(9)	TTL High
U706(4)	Low
U706(5)	TTL High
U706(6)	Low
U701(2)	Low
U701(5)	TTL High
U701(6)	Low

**Figure 7-23 RAM Bus Arbitrator Waveforms**



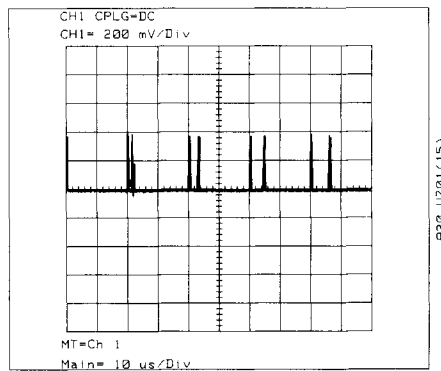
Probe: 10:1

Ch1: Connection- A30U707(14) " $\overline{\text{PBR}}$ "  
Coupling- dc  
Ground- Fourth Graticule From Top

Ch2: Connection- A30TP703 " $\overline{\text{PBG}}$ "  
Coupling- dc  
Ground- Second Graticule From Bottom

Trigger: Internal- Ch1  
Slope- Negative

Bandwidth Limit: OFF

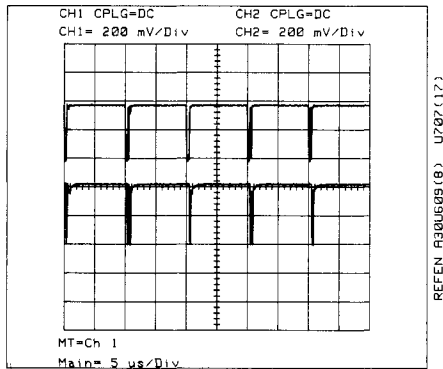


Probe: 10:1

Ch1: Connection- A30U701(15)  
Coupling- dc  
Ground- Center Graticule

Trigger: Internal- Ch1  
Slope- Positive

Bandwidth Limit: OFF



Probe: 10:1

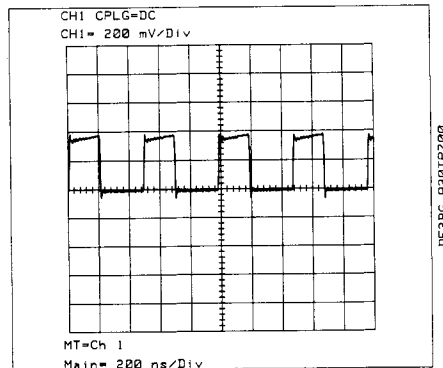
Ch1: Connection- A30U707(17)  
Coupling- dc  
Ground- Fourth Graticule From Top

Ch2: Connection- A30U609(8) "REFEN"  
Coupling- dc  
Ground- Third Graticule From Bottom

Trigger: Internal- Ch1  
Slope- Negative

Bandwidth Limit: OFF

Figure 7-24 DF3BG With DF3BR Grounded



Probe: 10:1

Ch1: Connection- A30TP700 "DF3BG"  
Coupling- dc  
Ground- Center Graticule

Trigger: Internal- Ch1  
Slope- Positive

Bandwidth Limit: OFF

**[A] RAM DATA BUS BUFFERS, [B] RAM ADDRESS SELECTOR, [D] MAIN RAM [J] RAM REFRESH COUNTER, [L] PROCESSOR/RAM DATA BUS INTERFACE [R] FFT/PROCESSOR INTERFACE, [U] RAM TEST PORT**

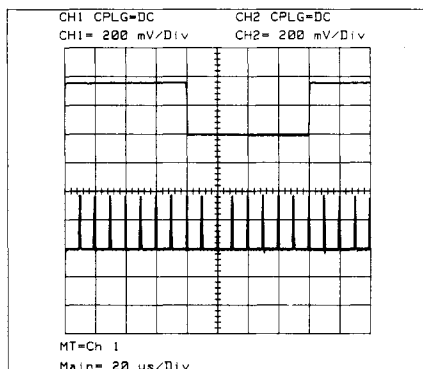
1. Turn the -hp-3561A LINE power switch OFF.
2. Remove the A20 Assembly and use a clip lead to short the two pins of A30W100 together.
3. Move test jumper A40W1 to the TEST position.
4. Turn the -hp-3561A LINE power switch ON.
5. When the "BLT TEST ROUTINE" message is displayed on the CRT, check the refresh counter waveforms given in Figure 7-25.

**NOTE**

*The A60 Assembly may be removed during this test to disable the beeper. However, this also disables the display so the "BLT TEST ROUTINE" message will not appear. The wave forms and signatures will be valid when the front panel LEDs begin to blink.*

6. Check the signatures given in Table 7-23 and 7-24 to troubleshoot the remaining RAM circuits and processor interface circuits.
7. When all of the waveforms and signatures have been checked, move jumper A40W1 back to the RUN position, re-insert the A20 Assembly, and remove the short from A30W100.

**Figure 7-25 RAM Refresh Counter Waveforms**



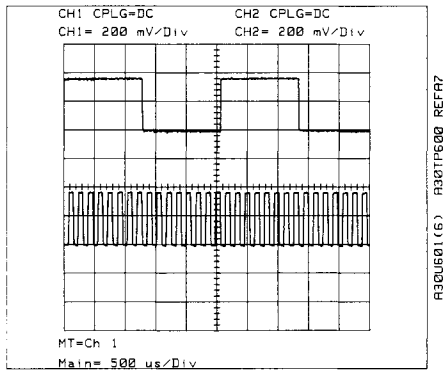
Probe: 10:1

Ch1: Connection- A30U601(6)  
Coupling- dc  
Ground- Third Graticule From Top

Ch2: Connection- A30U601(1) "REFEN"  
Coupling- dc  
Ground- Third Graticule From Bottom

Trigger: Internal- Ch1  
Slope- Positive

Bandwidth Limit: OFF



Probe: 10:1




Ch1: Connection- A30TP600 "REFA7"  
Coupling- dc  
Ground- Third Graticule From Top

Ch2: Connection- A30U601(6)  
Coupling- dc  
Ground- Third Graticule From Bottom

Trigger: Internal- Ch1  
Slope- Positive

Bandwidth Limit: OFF

**Table 7-23 RAM Address and Data Bus Signatures**

<b>Signature Analyzer Setup</b>			
<b>Signal</b>	<b>Polarity</b>	<b>Connection</b>	
Clock		A30TP703 "PBG"	
Start		A40J100(5)	
Stop		A40J100(4)	
+ 5 V Signature - 5UAH			
<b>Processor/RAM Data Bus Interface (write to RAM)</b>		<b>RAM Address Selector</b>	
U502(3)	70H0	U200(4)	2525
U502(5)	0C43	U200(7)	0476
U502(7)	00A2	U200(9)	UACC
U502(9)	515U	U200(12)	P76P
U502(12)	C8H3		
U502(14)	F61C	U205(4)	265H
U502(16)	929C	U205(7)	5U5P
U502(18)	AFU0	U205(9)	2134
		U205(12)	CC17
U506(3)	AP35		
U506(5)	F680		
U506(7)	HAU4		
U506(9)	F15A		
U506(12)	118F		
U506(14)	276U		
U506(16)	5165		
U506(18)	354A		
<b>RAM Data Bus Buffers (write to RAM)</b>			
U604(2)	H058		
U604(3)	2133		
U604(4)	UU2A		
U604(5)	9C1H		
U604(6)	A4UA		
U604(7)	0U28		
U604(8)	49UH		
U604(9)	PPHF		
U700(2)	U68P		
U700(3)	POP2		
U700(4)	9621		
U700(5)	H2HP		
U700(6)	518H		
U700(7)	F80A		
U700(8)	2HAH		
U700(9)	24F4		

**Table 7-23 RAM Address and Data Bus Signatures (Cont'd)**

Signal	Polarity	Connection
Clock		A30TP703 "PBC"
Start		A40J100(5)
Stop		A40J100(4)
+ 5 V Signature - 5UAH		
Main RAM		Processor/Ram Bus Interface (Read from RAM)
U201(2)	6CAC	U501(2) 35H5
U202(2)	6890	U501(5) F433
U203(2)	4168	U501(6) A0C4
U204(2)	899A	U501(9) C4C6
U207(2)	AAF8	U501(12) F925
U208(2)	U6U6	U501(15) 225P
U209(2)	5216	U501(16) H48P
U210(2)	17CF	U501(19) 027H
U300(2)	924A	U505(2) H564
U301(2)	A44A	U505(5) 7C7C
U302(2)	49PA	U505(6) A90C
U303(2)	04UA	U505(9) 0CHP
U306(2)	H0A2	U505(12) 182A
U307(2)	6U6U	U505(15) 47FF
U308(2)	91HU	U505(16) C894
U309(2)	FF67	U505(19) 6633

**Table 7-24 FFT/Processor Interface Signatures**

Signal	Polarity	Connection
Clock		A30TP601 "RIOS"
Start		A40J100(5)
Stop		A40J100(4)
+ 5 V Signature - H7PC		
FFT/Processor Interface		
U600(2)	F6F0	
U600(3)	112C	
U600(7)	HPH1	
U600(10)	P376	
U600(14)	F6F0	
U606(15)	7F2P	

**[D] MAIN RAM**

If the signatures given in Table 7-23 are correct, the power on test can be used to isolate RAM failures to the component. When the power on test encounters a RAM failure, it lists return code 0 7 26 and a chip code. Table 7-25 lists the chip codes and the corresponding failed RAM.

**Table 7-25 Power on Test RAM failures**




Return code - 0 7 26	
Chip code	Failed RAM
0	U201
1	U202
2	U203
3	U204
4	U205
5	U300
6	U301
7	U302
8	U303
9	U207
A	U208
B	U209
C	U210
D	U307
E	U308
F	U309

**[O] FFT PROCESSOR, [Q] FFT INSTRUCTION ROM**

1. Turn the -hp-3561A LINE power switch OFF.
2. Move test jumpers A30W101 and A30W102 to the test position. Use a clip lead to short the two pins of A30W100 together.
3. Turn the -hp-3561A LINE power switch ON and check the signatures given in Table 7-26.
4. When all of the signatures have been checked, move jumpers A30W101 and A30W102 back to the NORM position and remove the short from A30W100.



**Table 7-26 FFT Processor and ROM Signatures**

Signal	Polarity	Connection
Clock		A30J1(3)
Start		A30J1(5)
Stop		A30J1(4)
+ 5 V Signature - 7A70		
FFT Processor Address Bus		FFT Address Bus Buffers
U100(1)	C21A	U4(3) H62U
U100(2)	H62U	U4(5) C21A
U100(27)	0000	U4(7) HA07
U100(28)	8P54	U4(9) H0AA
U100(29)	1734	U4(12) P030
U100(34)	9635	U4(14) 4442
U100(35)	0772	U4(16) 4U2A
U100(36)	4U2A	U4(18) 0772
U100(37)	4442	
U100(38)	P030	U7(3) 9635
U100(39)	H0AA	U7(5) 1734
U100(40)	HA07	U7(7) 8P54
		U7(9) 0000
FFT Instruction ROM		
U400(9)	HP00	
U400(10)	HP01	
U400(11)	HP02	
U400(13)	HP03	
U400(14)	HP04	
U400(15)	HP05	
U400(16)	HP06	
U400(17)	HP07	
U402(9)	HP08	
U402(10)	HP09	
U402(11)	HP10	
U402(13)	HP11	
U402(14)	HP12	
U402(15)	HP13	
U402(16)	HP14	
U402(17)	HP15	

**Table 7-27 A30 Assembly Signal Connections**

**INPUTS**

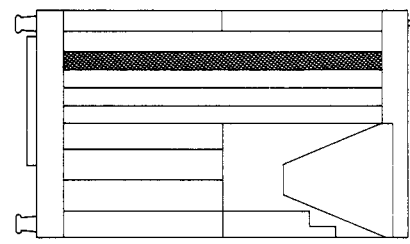
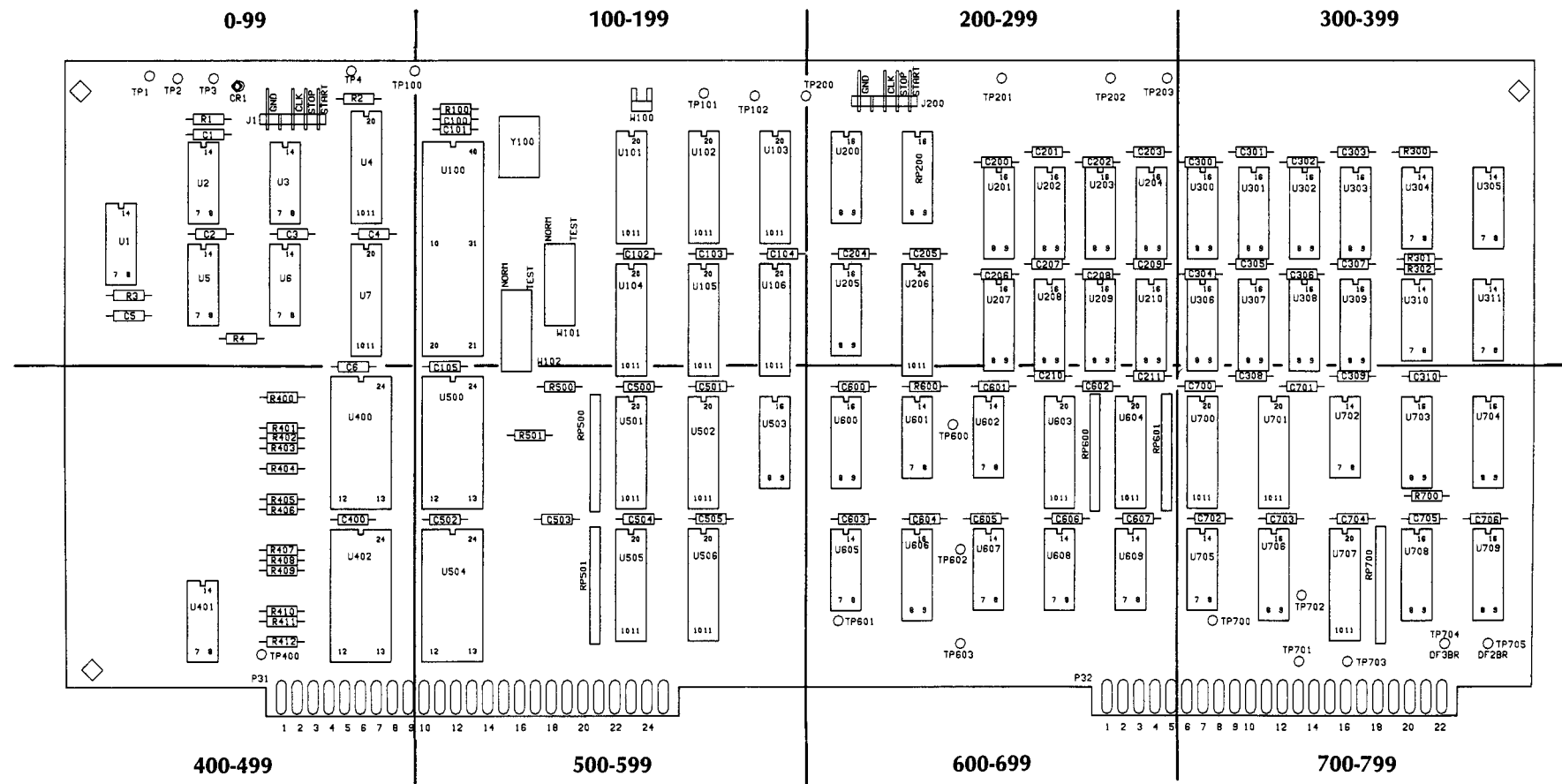
Signal Name	Functional Block	Connector Number	Origin Assembly
<u>DF1BR</u>	H	P32(A12)	A20
<u>DF2BR</u>	H	P32(A13)	A20
<u>DF3BR</u>	H	P32(A14)	A20
<u>PBLDS</u>	F	P31(A6)	A40
<u>PBR</u>	H	P32(A16)	A40
<u>PBR/W</u>	K	P32(B7)	A40
<u>PBUDS</u>	F	P31(B6)	A40
<u>PRAMRE</u>	L	P31(A7)	A40
<u>PRIOS</u>	I	P32(B17)	A40
<u>RESET</u>	R	P31(B3)	A40
100 kHz	G	P31(B2)	A40
20.48 MHz	C	P31(A2)	A40

**OUTPUTS**

Signal Name	Functional Block	Connector Number	Destination Assembly
<u>DF1BC</u>	I	P32(B12)	A20
<u>DF2BC</u>	I	P32(B13)	A20
<u>DF3BC</u>	I	P32(B14)	A20
<u>FFTI</u>	S	P31(B4)	A40
<u>PBG</u>	I	P32(B16)	A40
<u>RBR/W</u>	K	P31(B16)	A20
<u>RIOS</u>	K	P31(A16)	A20

**I/O SIGNALS**

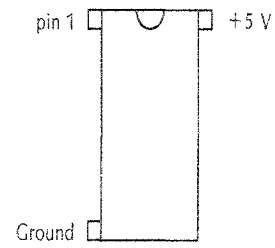
Signal Name	Functional Block	Connector Number	Destination Assembly
RAM Address Bus RAB0 - RABF	B	P31(A17 - A24) P31(B17 - B24)	A20, A40
RAM Data Bus RDB0 - RDBF	L	P32(A4 - A11) P32(B4 - B11)	A20
Processor Data Bus PDB0 - PDBF	L	P31(A8 - A15) P31(B8 - B15)	A40, A50, A60, A65/66



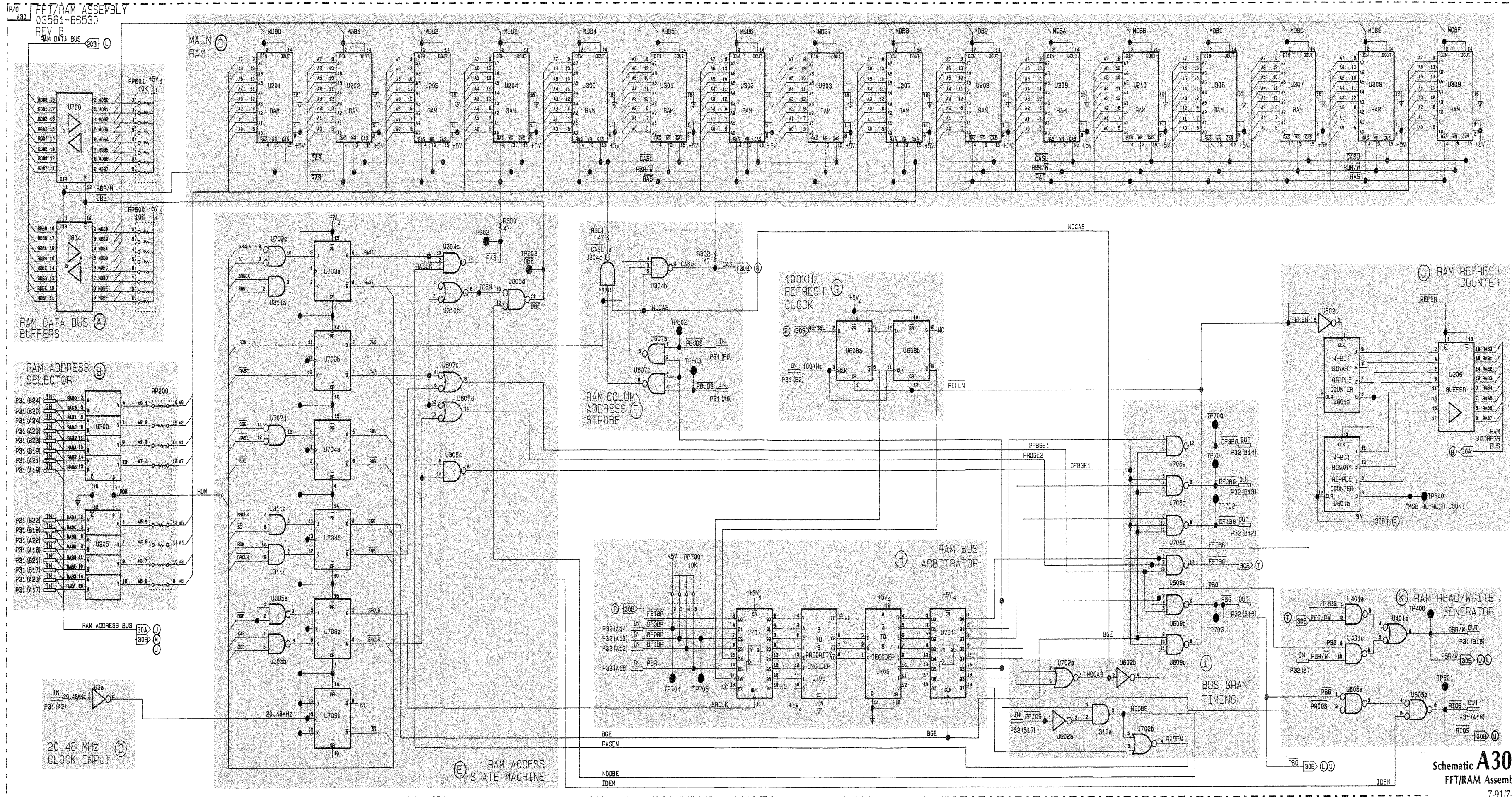
A30 Assembly

All integrated circuits are corner powered except those shown in the table below. Corner powered ICs have ground connected to the lower left pin, and +5 V connected to the upper right pin regardless of the total pin count. (eg, for a 16 pin DIP, ground is connected to pin 8 and +5 V is connected to pin 16)

Corner Power

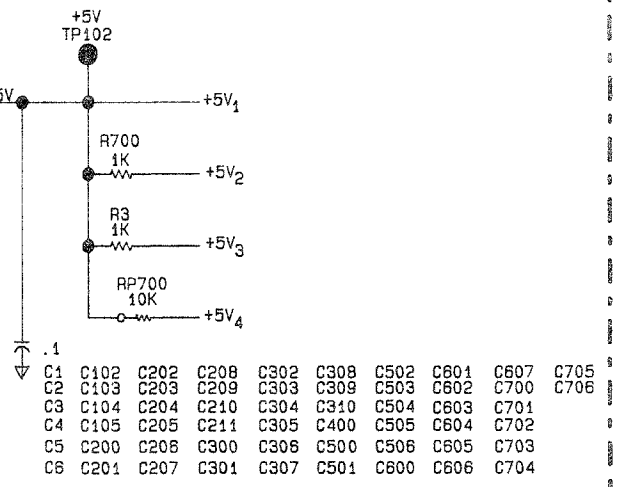
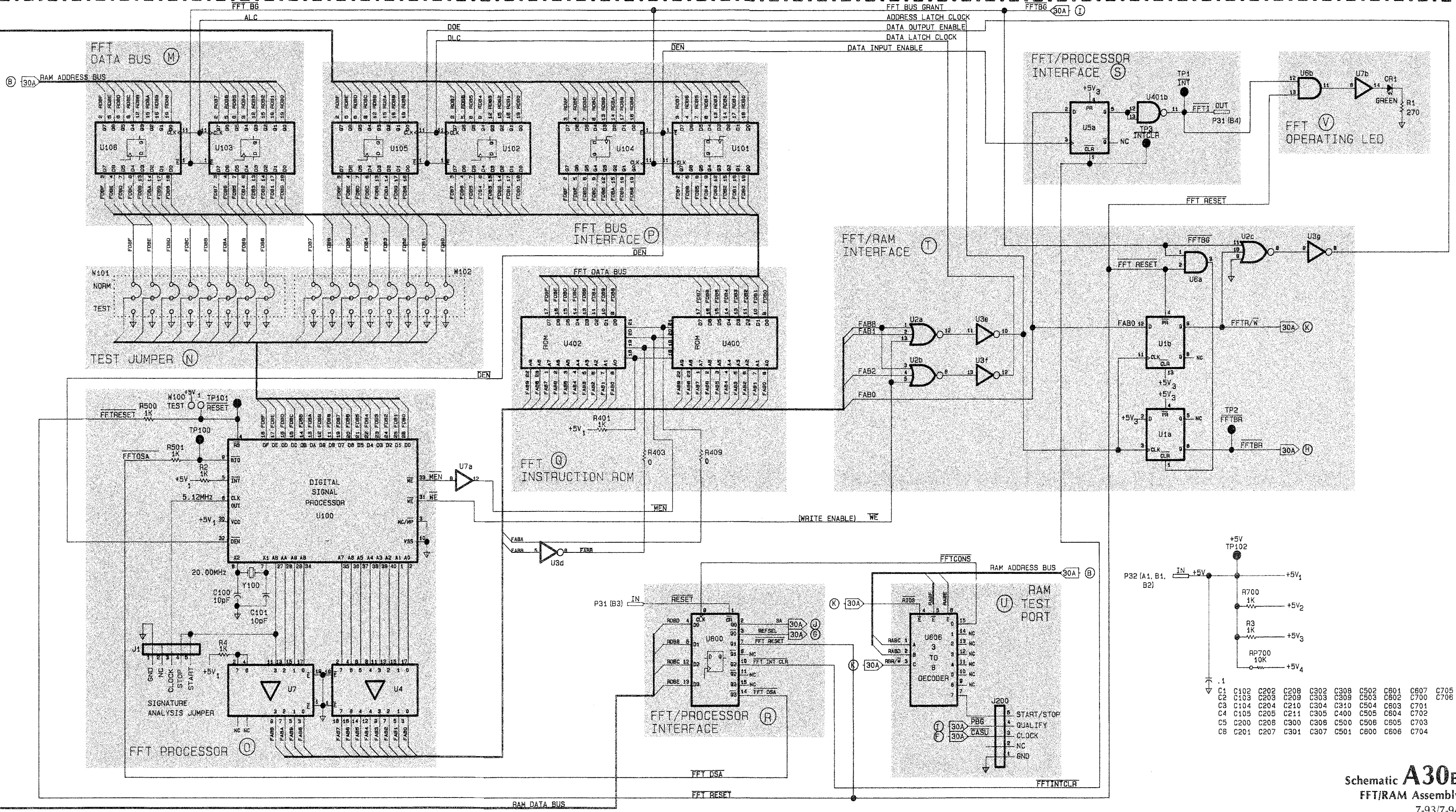
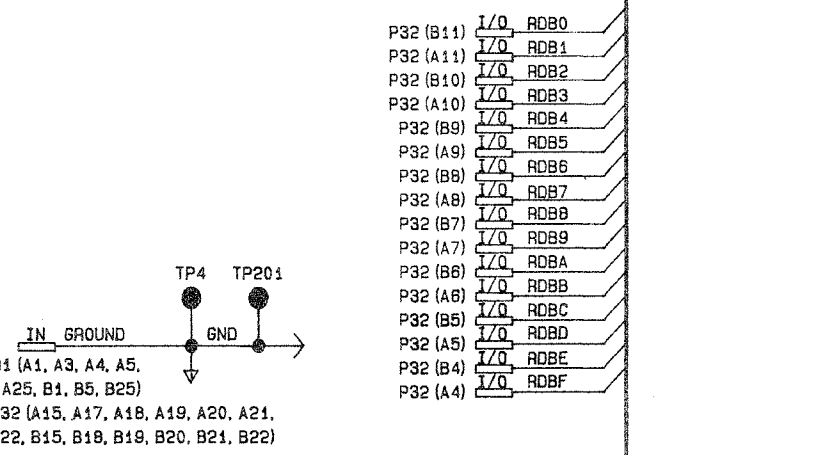
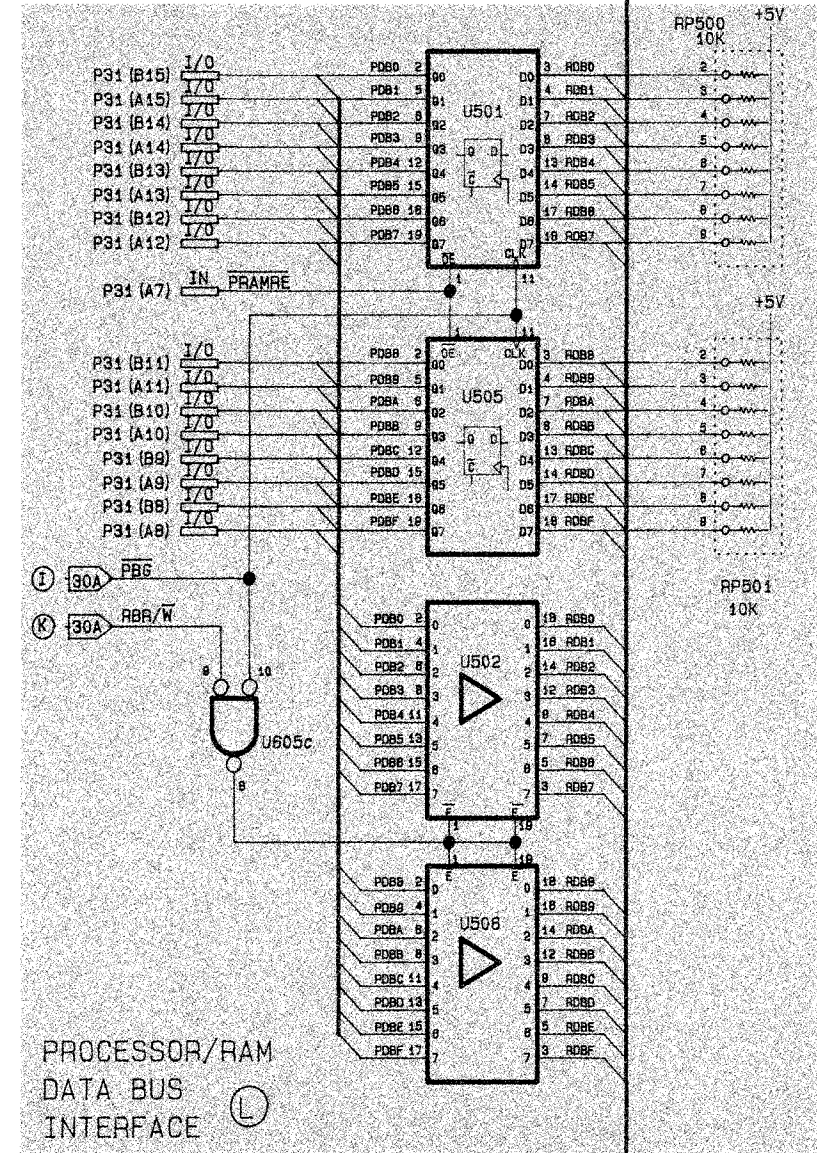


	+5V	GND
U100	30	10
U201	8	16
U202	8	16
U203	8	16
U204	8	16
U207	8	16
U208	8	16
U209	8	16
U210	8	16
U300	8	16
U301	8	16
U302	8	16
U303	8	16
U304	8	16
U305	8	16
U306	8	16
U307	8	16
U308	8	16
U309	8	16





P/O A30 FFT/RAM ASSEMBLY  
03561-66530  
REV B



Schematic A30B  
FFT/RAM Assembly  
7-93/7-94

## **7-16 A40 PROCESSOR/ROM ASSEMBLY**

### **7-17 Processor/ROM Circuit Description**

#### **GENERAL**

The main function of the microprocessor assembly is instrument control. Through the processor data bus, address bus, and I/O select lines, the microprocessor sets up and controls most circuits in the -hp-3561A and through the processor interrupt lines, these circuits can access the microprocessor. Together all of these signals allow the processor to direct the activity required for the -hp-3561A to take, process, and display measurement data. In addition to the microprocessor, ROM, and I/O control circuitry, the A40 Assembly contains the master 20.48 MHz clock, which determines the frequency accuracy of the instrument.

#### **[A] INTERRUPT PRIORITY ENCODER, [K] INTERRUPT VECTOR GENERATOR**

When an interrupt is received by the priority interrupt encoder, it compares the priority of the interrupt with the priority of any other active interrupts (level 7 in U408 being the highest level and level 0 the lowest). It then issues the highest priority interrupt to the processor where an interrupt acknowledge cycle is initiated. In this cycle the processor outputs the binary interrupt level on the first three address lines PA0, PA1, and PA2, and issues an interrupt acknowledge signal,  $\overline{\text{PINTA}}$ .  $\overline{\text{PINTA}}$  latches the first three address lines in the interrupt vector generator. The processor next reads the vector generator to determine the location in memory of the interrupt service routine.

#### **[I] RAM BUS INTERFACE HANDSHAKE, [B] RAM BUS INTERFACE BUFFER**

To access the instrument RAM, the processor must issue a bus request ( $\overline{\text{PBR}}$ ) to the RAM bus arbitrator. If the processor bus request is the highest priority request, the RAM bus arbitrator will issue a bus grant to the processor. On receipt of a bus grant, the processor places an address and data onto the RAM address and data bus respectively. The RAM bus interface then clears the bus request, and issues a  $\overline{\text{RAMH}}$  signal to complete the RAM bus cycle.

**[D] MICROPROCESSOR**

The central microprocessor is a 68000, 16 bit processor. It communicates with peripheral circuits through the processor address bus and processor data bus, using the address strobe, data strobe, and the data acknowledge signals to coordinate the data transfer. Address strobe,  $\overline{AS}$ , goes low to indicate that the address is valid on the processor address bus. Upper data strobe,  $\overline{PUDS}$ , and lower data strobe,  $\overline{PLDS}$ , go low to indicate that data is valid on the upper 8 bits and lower 8 bits of the data bus respectively. A processor bus cycle is terminated by the data acknowledge signal,  $\overline{DTACK}$ .

**[H] ADDRESS STROBE TIMING DELAY, [J] DATA ACKNOWLEDGE GENERATOR**

The address strobe timing delay circuit delays the address strobe signal to account for address delays through the bus buffers. Delayed address strobe,  $\overline{DAS}$  is delayed by one clock cycle, and is used for addressing circuits on the A40 Assembly. The address strobe signal is further delayed to account for the communication time to the ROM, noise source, and front panel.

The delayed address strobe signals are used by the data acknowledge generator to determine the length of a bus cycle to any particular peripheral. The data acknowledge generator reads the address bus to determine which peripheral the processor is talking to. This address is then used to select the appropriate delayed address strobe to generate the  $\overline{DTACK}$  signal. All bus cycle times are fixed by the delayed address strobe signals except RAM access and display access. The data acknowledge generator depends on a response from these two circuits to generate a  $\overline{DTACK}$ .  $\overline{RAMH}$  indicates that the RAM bus cycle is complete and  $\overline{DSPH}$  indicates that a display bus cycle is complete.

**[M] I/O ADDRESS DECODING, [L] CONTROL AND ADDRESS BUS BUFFER**

The processor address bus is partially decoded on the A40 Assembly by the I/O address decoder. This circuit generates a select signal for each major circuit in the instrument. The processor address bus and the data bus strobe are buffered through the control and address bus buffer and sent to the peripheral circuits where the address is further decoded to a particular device within the selected circuit.

**[Q] POWER-ON RESET**

The LOW +5 signal from the power supply holds the processor in reset until the +5 volt supply is fully operational at power on. The RESET and HALT signals are bi-directional and can be driven by either the processor or the power on reset circuit to reset the -hp-3561A. The two pins of the RESET test point (TP2) may be shorted together to manually reset the processor.

**[T] WATCH DOG TIMER**

This circuit will reset the processor if the processor does not access the front panel every ten micro seconds. This should only occur in the case of a failure. The watch dog timer may be disabled by jumper A40W3.

**[P] ROM, [O] ROM ADDRESS DECODING**

The processor executes the instructions stored in the ROM. The ROM address consists of two parts, the ROM chip select signals address a ROM chip while the address bus addresses the location within the selected ROM. The power on self test is stored in ROMS #1 and #2 (U502, U106) If these ROMs have failed, the power on test will not run. Using the power up test program stored in ROM #1, the processor can check the integrity of the other ROMs.

**[R] CLOCK GENERATOR, [S] CLOCK DIVIDE  $\div 10 \div 100$** 

In addition to the microprocessor circuits, this oscillator provides a clock signal to the following circuits: Noise Source (A50), CMOS and Bubble Memory (A66/65).

**[U] 20.48 MHz CRYSTAL OSCILLATOR, [V] CLOCK OUTPUT BUFFER**

This oscillator provides a clock signal for the following circuits: RAM (A30), Digital Filter (A20), Power Supply (A70), A/D Converter (A15). The accuracy of this oscillator determines the overall frequency accuracy of the instrument.



**Table 7-28 A40 Assembly Signal Descriptions**

Signal	Description
$\overline{AS}$	Address Strobe: This signal goes low once per processor bus cycle to indicate that data is valid on the processor address bus.
$\overline{BERR}$	Bus ERRor: This signal goes low to abort the current bus cycle. The $\overline{BERR}$ signal is activated if the bus cycle takes longer than expected.
$\overline{BUBI}$	BUBble memory Interrupt: The bubble memory uses this signal to request service from the processor.
$\overline{CMOSS}$	CMOS memory Select: Addresses the CMOS memory on the A65/66 Assembly for processor access.
$\overline{DAS}$	Delayed Address Strobe: Address strobe delayed by one 8 MHz clock cycle.
$\overline{DINT}$	Data acknowledge INTerrupt: Forces a $\overline{DTACK}$ to indicate to the processor that the interrupt vector has been latched.
$\overline{DMAI}$	Direct Memory Access Interrupt: Tells the processor that the digital filter has processed a complete time record and stored the result in RAM.
$\overline{DSPH}$	DiSPlay Holdoff: This signal holds off the $\overline{DTACK}$ signal until the display access is complete.
$\overline{DSPS}$	DiSPlay Select: Addresses the display for processor access.
$\overline{DTACK}$	DaTa ACKnowledge: This signal goes low to indicate to the processor that the current bus cycle is complete.
$\overline{FFTI}$	FFT Interrupt: The FFT uses this signal to indicate that the FFT is complete, and the results are available for further processing or display.
$\overline{FIOH}$	Fast I/O Holdoff: This signal holds off the $\overline{DTACK}$ signals by four 8 MHz clock cycles for all fast I/O port bus cycles.
$\overline{FPS}$	Front Panel Select: Addresses the front panel for processor access.
$\overline{HALT}$	Processor HALT: This signal goes low to indicate that the processor is not executing instructions. The red LED, CR2, illuminates when $\overline{HALT}$ is low. This signal may be driven low by either the processor or the reset circuit.
$\overline{HPCI}$	HP-IB Control Interrupt: Used for all HP-IB activity except binary data transfer.
$\overline{HPDI}$	HP-IB Data Interrupt: A faster interrupt used for binary data transfer only.
$\overline{HPIBS}$	HP-IB Select: Addresses the HP-IB circuit on the A50 Assembly for processor access.

**Table 7-28 A40 Assembly Signal Descriptions (Cont'd)**

Signal	Description
$\overline{\text{IOPORT\#7}}$	I/O PORT Number 7: The processor addresses this port to clear the interrupt vector generator.
$\overline{\text{LOS}}$	Local Oscillator Select: Addresses the local oscillator on the A50 Assembly for processor access.
LOW + 5	LOW + 5 Volt Supply: At power on this signal is held low until the + 5 V signal is fully operational.
PA0 - PAF	Processor Address bus 0-F (16 bit hex): Buffered processor address bus.
PA17 PA18 PA19	Processor Address Bus: Address lines used only for circuits on the A40 Assembly.
PD0 - PDF	Processor Data Bus 0-F (16 bit hex): Buffered processor data bus.
$\overline{\text{PINTA}}$	Processor INTerrupt Acknowledge: This signal goes low at the start of an interrupt acknowledge bus cycle to latch the interrupt vector.
$\overline{\text{PLDS}}$	Processor Lower 8 bit Data Strobe: Indicates that the lower 8 bits (PD0 - PD7) of the processor data bus are valid.
$\overline{\text{PRAMRE}}$	Processor RAM REad: Goes low to tell the RAM that the current bus cycle is a read operation.
$\overline{\text{PRIOS}}$	Processor Ram I/O Select: High when the processor is accessing the RAM and low when the processor is accessing an I/O port through the RAM bus.
$\overline{\text{PUDS}}$	Processor Upper 8 bit Data Strobe: Indicates that the upper 8 bits (PD8 - PDF) of the processor data bus are valid.
$\overline{\text{PWRFAIL}}$	PoWeR FAIL Interrupt: Indicates a power fail condition to the processor.
$\overline{\text{RESET}}$	RESET: This signal is goes low to reset the processor and the entire instrument. $\overline{\text{RESET}}$ can be controlled by either the processor or the reset circuit.
RAB0 - RABF	RAM Address Bus $\overline{0 - F}$ (16 bit hex): Addresses the RAM and I/O ports tied to the RAM bus when a $\overline{\text{PBG}}$ is issued from the RAM bus arbitrator.
RCS0 - RCS11	ROM Chip Select 0 through 11: These signals select the ROM Chip to be addressed by the address bus.
$\overline{\text{SINT}}$	Noise Source INTerrupt: This signal goes low when the noise source needs to be re-armed.
$\overline{\text{TINT}}$	Timer INTerrupt: Indicates to the processor that the watch dog timer is about to issue a RESET.

## 7-18 Troubleshooting the Processor/ROM

### GENERAL

Failures on the A40 Assembly will generally cause the instrument to fail the power up test in some way. It is useful to separate these failures into the two categories listed below.

- 1) Instrument "hangs up" and does not complete the power up test.
- 2) Instrument completes the power up test with a return code.

Troubleshoot the circuits on the A40 Assembly in the order given in Table 7-29. In this table, level one circuits must be operational before level two circuits can be tested and so on. Instrument "hang up" failures usually indicate level one through four circuits, while return code failures usually indicate level five or six failures.

### NOTE

*To disable the beeper, the A60 Assembly can be removed while troubleshooting the A40 Assembly. Removing the A60 Assembly also disables the display.*

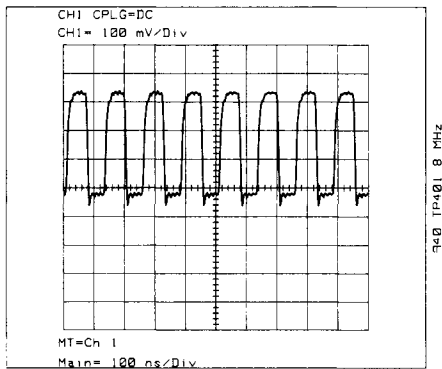
**Table 7-29 A40 Circuit Troubleshooting Order**

LEVEL	Functional Blocks
1	Clock: R Power on Reset: Q
2	Clock Divider: S
3	Interrupt Priority Encoder: A
4	Microprocessor: D Address Strobe Delay: H Data Acknowledge Generator: J Processor Data Bus: G Bus Error Detector: E
5	Processor Address Bus: C, B Power Up Test ROMs: P
6	All other circuits on the A40 Assembly

### [R] CLOCK

Check the clock waveforms at test point A40TP401 and test point A40TP402 given in Figure 7-26.

Figure 7-26 A40 Clock Waveforms

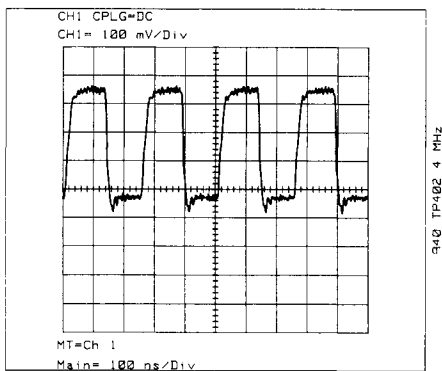


Probe: 10:1

Ch1: Connection- A40TP401 "8 MHz"  
Coupling- dc  
Ground- Center Graticule

Trigger: Internal- Ch1  
Slope- Positive

Bandwidth Limit: OFF



Probe: 10:1

Ch1: Connection- A40TP402 "4 MHz"  
Coupling- dc  
Ground- Center Graticule

Trigger: Internal- Ch1  
Slope- Positive

Bandwidth Limit: OFF

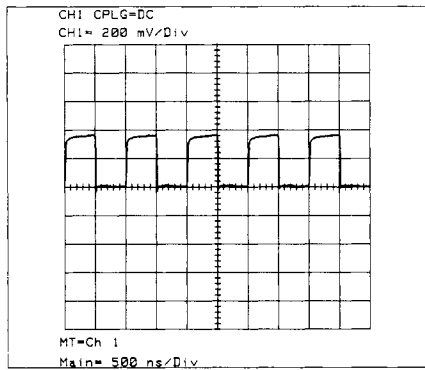
### [Q] POWER ON RESET

1. Move test jumper A40W3 to the test position.
2. Short the two pins of the reset test point (TP2) together.
3. Check the  $\overline{\text{RESET}}$  signal and the  $\overline{\text{HALT}}$  signal at U6(18) and U6(17). Both of these should be TTL low.
4. Remove the short from the reset test point (TP2) and re-check  $\overline{\text{RESET}}$  and  $\overline{\text{HALT}}$  signals. These signals should now be TTL high.
5. Move test jumper A40W3 to the normal position.

**[S] CLOCK DIVIDER, [A] INTERRUPT PRIORITY ENCODER**

1. Turn the -hp-3561A LINE power switch OFF and move test jumper A40W2 to the test position.
2. Turn the -hp-3561A LINE power switch ON and check the waveforms given in Figure 7-27.
3. Move test jumper A40W2 to the normal position.

**Figure 7-27 Clock Divider and Interrupt Waveforms**

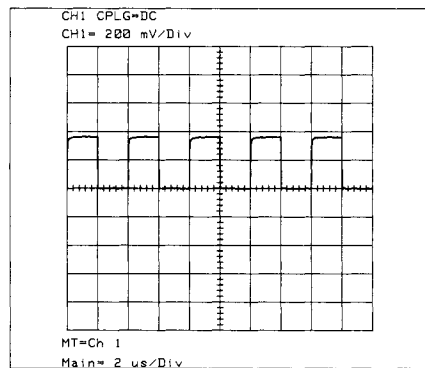


Probe: 10:1

Ch1: Connection- A40U4(4) "1 MHz"  
Coupling- dc  
Ground- Center Graticule

Trigger: Internal- Ch1  
Slope- Positive

Bandwidth Limit: OFF

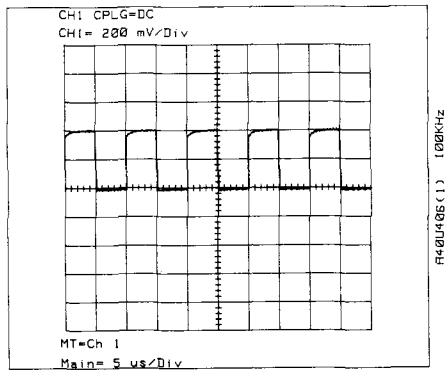


Probe: 10:1

Ch1: Connection- A40U4(6) "250 kHz"  
Coupling- dc  
Ground- Center Graticule

Trigger: Internal- Ch1  
Slope- Positive

Bandwidth Limit: OFF

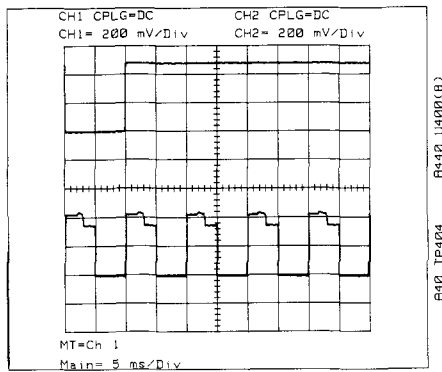


Probe: 10:1

Ch1: Connection- A40U406(1) "100 kHz"  
Coupling- dc  
Ground- Center Graticule

Trigger: Internal- Ch1  
Slope- Positive

Bandwidth Limit: OFF



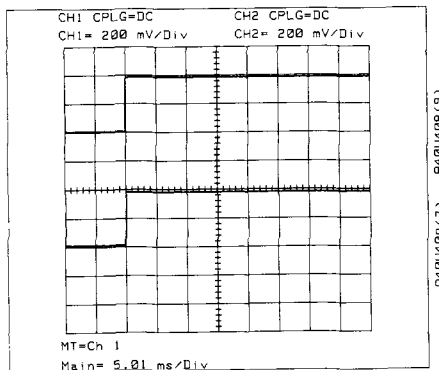
Probe: 10:1

Ch1: Connection- A40U400(8) "TINT"  
Coupling- dc  
Ground- Third Graticule From Top

Ch2: Connection- A40TP404 "100 Hz"  
Coupling- dc  
Ground- Third Graticule From Bottom

Trigger: Internal- Ch1  
Slope- Negative

Bandwidth Limit: OFF



Probe: 10:1

Ch1: Connection- A40U408(9)  
Coupling- dc  
Ground- Third Graticule From Top

Ch2: Connection- A40U408(7)  
Coupling- dc  
Ground- Third Graticule From Bottom

Trigger: Internal- Ch1  
Slope- Negative

Bandwidth Limit: ON

**[D] MICROPROCESSOR, [H] ADDRESS STROBE TIMING DELAY, [J] DATA ACKNOWLEDGE GENERATOR, [E] BUS ERROR DETECTOR**

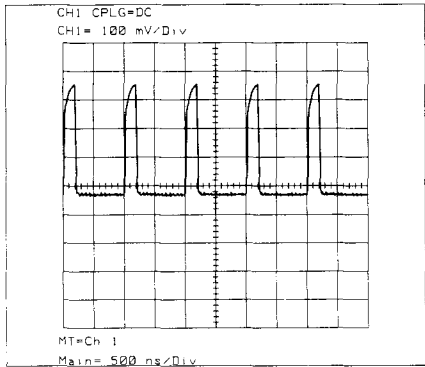
These circuits form the basic processor bus cycle loop. A failure in any one of these circuits will cause the the processor to lock up and all of the signals will go to a static state. The basic processor loop consists of U3, U4, U8, U9, U405, U409 and the microprocessor itself U6.

1. Turn the -hp-3561A LINE power switch OFF and move test jumpers A40W2 and A40W3 to the test position.
2. Turn the -hp-3561A LINE power switch ON and check the processor input signals listed in Table 7-30. All of these signals must be correct before proceeding with the next step.
3. Check the waveforms given in Figure 7-28.
4. If all of these signals are stuck in a static state, replace U3 and re-check the waveforms given in Figure 7-28. Repeat this process for U4, U8, U9, U405, and U409. If the processor loop test is still failing, the failure is most likely in the processor itself, replace U6.

**Table 7-30 Processor Loop Test Input Signals**

Signal Name	Signal Position	Signal State (TTL Level)
	U402(8)	high
	U401(11)	low
	U403(11)	high
<u>BERR</u>	U6(22)	high
<u>HALT</u>	U6(17)	high
<u>RESET</u>	U6(18)	high
D0	U6(5)	low
D1	U6(4)	high
D2	U6(3)	high
D3	U6(2)	high
D4	U6(1)	high
D5	U6(64)	high
D6	U6(63)	high
D7	U6(62)	high
D8	U6(61)	low
D9	U6(60)	high
D10	U6(59)	high
D11	U6(58)	high
D12	U6(57)	high
D13	U6(56)	high
D14	U6(55)	high
D15	U6(54)	low

Figure 7-28 Processor Loop Test Waveforms



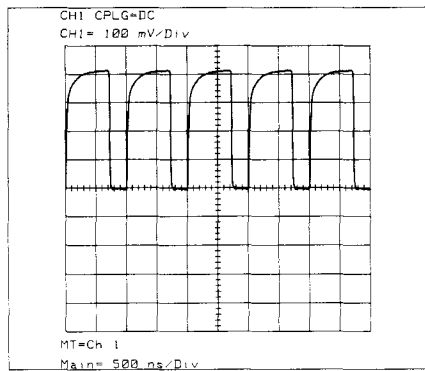
Probe: 10:1

Ch1: Connection- A40J100(3) "AS"  
 A40U6(8) "PLDS"  
 A40U6(7) "PUDS"

Coupling- dc  
 Ground- Center Graticule

Trigger: Internal- Ch1  
 Slope- Positive

Bandwidth Limit: ON

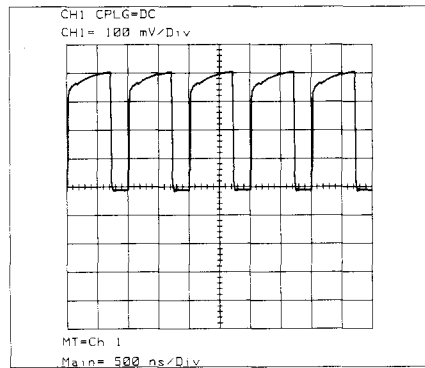


Probe: 10:1

Ch1: Connection- A40U8(3) "DAS"  
 Coupling- dc  
 Ground- Center Graticule

Trigger: Internal- Ch1  
 Slope- Positive

Bandwidth Limit: ON

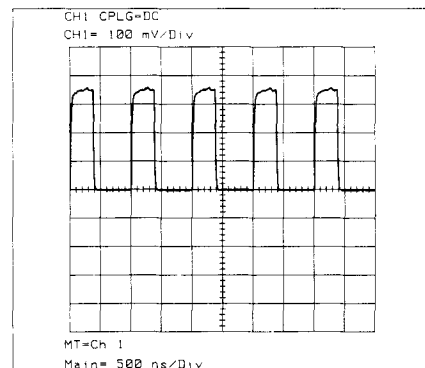


Probe: 10:1

Ch1: Connection- A40TP4 "DTACK"  
 Coupling- dc  
 Ground- Center Graticule

Trigger: Internal- Ch1  
 Slope- Positive

Bandwidth Limit: ON



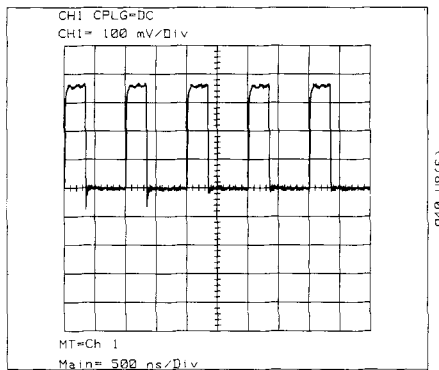
Probe: 10:1

Ch1: Connection- A40U3(9) "ROMH"  
 Coupling- dc  
 Ground- Center Graticule

Trigger: Internal- Ch1  
 Slope- Positive

Bandwidth Limit: ON





Probe: 10:1

Ch1: Connection- A40U8(6) "FIOH"  
Coupling- dc  
Ground- Center Graticule

Trigger: Internal- Ch1  
Slope- Positive




Bandwidth Limit: OFF

**[C] PROCESSOR ADDRESS BUS, [O] ROM ADDRESS DECODERS, [P] POWER UP TEST ROM, [G] PROCESSOR DATA BUS**




The power up test software is stored in the first two ROMs, U106 and U502. These ROMs must be operational before the power up test can be run. This test checks all of the circuits used to address and read data from the first two ROMs. All other ROM failures are detected through return codes in the power up test.

1. Turn the -hp-3561A LINE power switch OFF and move test jumpers A40W2 and A40W3 to the test position.
2. Turn the -hp-3561A LINE power switch ON and check the signatures given in Table 7-31.

**Table 7-31 A40W2 Test Signatures**

Signature Analyzer Setup		
Signal	Polarity	Connection
CLOCK		J100(3) "AS"
START		J100(5)
STOP		J100(4)
+ 5 V Signature - 00UP		
Processor Address Bus		Processor Address Bus Buffers
U6(29)	0055	U500(3) PPP1
U6(30)	0033	U500(5) H42C
U6(31)	000U	U500(7) 000U
U6(32)	UUUU	U500(9) 0055
U6(33)	H42C	U500(12) 0033
U6(34)	4074	U500(14) UUUU
U6(35)	PPP1	U500(16) 4074
U6(36)	89F1	U500(18) 89F1
U6(37)	31PC	
U6(38)	34C1	U503(3) P625
U6(39)	15HU	U503(5) U540
U6(40)	7U42	U503(7) 9C51
U6(41)	PC1A	U503(9) PC1A
U6(42)	9C51	U503(12) 7U42
U6(43)	U540	U503(14) 15HU
U6(44)	P625	U503(16) 31PC
U6(45)	0055	U503(18) 34C1
U6(46)	0033	
U6(47)	000U	
ROM Address Decoding		
U605(7)	60FF	
U605(9)	3700	
U605(10)	6935	
U605(11)	3PC9	
U605(12)	FO9A	
U605(13)	6U02	
U605(14)	H369	
U605(15)	7F70	
U606(7)	18U2	
U606(9)	4H01	
U606(10)	9A8F	
U606(11)	FU6U	
U606(12)	30P7	
U606(13)	9C01	
U606(14)	341C	
U606(15)	9UHH	

**Table 7-31 A40W/2 Test Signatures (Cont'd)**

Power on Test ROMs (U106, U502) and Processor Data Bus			
Signature Analyzer Setup			
Signal	Polarity	Connection	
CLOCK		TP501 "RCS0"	
START		J100(5)	
STOP		J100(4)	
+ 5 V Signature - 1180			
U106(11)	1H75	U502(11)	1PU7
U106(12)	4PP8	U502(12)	A506
U106(13)	1180	U502(13)	47CF
U106(15)	AC06	U502(15)	01P8
U106(16)	H161	U502(16)	3C9C
U106(17)	AP7C	U502(17)	9C3A
U106(18)	A6CP	U502(18)	771A
U106(19)	19AS	U502(19)	A33F

**[P] ROM**

If all tests to this point have passed, the -hp-3561A power up test will be operational. To check the remaining ROMs run the power up test. The return codes and corresponding failed ROMs are listed in Table 7-32.

**Table 7-32 Power-on Test ROM Return Codes**




Return Code	Failed ROM
0 1 01	U502
0 1 02	U106
0 1 03	U600
0 1 04	U200
0 1 05	U601
0 1 06	U201
0 1 07	U602
0 1 08	U202
0 1 09	U603
0 1 10	U203
0 1 11	U700
0 1 12	U302
0 1 13	U701
0 1 14	U303
0 1 15	U702
0 1 16	U304
0 1 17	U703
0 1 18	U305
0 1 19	U704
0 1 20	U306
0 1 21	U301
0 1 22	U300
0 1 23	U708
0 1 24	U707

**[B] RAM ADDRESS BUS INTERFACE BUFFER, [G] DATA BUS BUFFERS, [L] CONTROL AND ADDRESS BUS BUFFER, [I/O ADDRESS DECODING**

This test uses signature analysis to check most of the A40 Assembly I/O signals. Because this test depends only on the power supply and the processor assembly itself, any of the other assemblies can be removed without affecting the test results. If the test fails, assemblies A20, A30, A50, A60, and A65 can be removed and the test re-run to determine if one of these assemblies is loading down the A40 I/O signals.

1. Turn the -hp-3561A LINE power switch OFF and move test jumpers A40W2 and A40W3 to the test position.
2. Turn the -hp-3561A LINE power switch ON and check the signatures given in Table 7-33.
3. Turn the -hp-3561A LINE power switch OFF. Move test jumpers A40W2 and A40W3 back to the run position, and move test jumper A40W1 to the test position.
4. Turn the -hp-3561A LINE power switch ON. When the front panel LEDs begin to blink ( $\approx 10$  seconds after power-on), check the signatures given in Table 7-34.

**Table 7-33 Processor I/O and Address Bus Signatures**

Signature Analyzer Setup			
Signal	Polarity	Connection	
CLOCK		J100(3) "AS"	
START		J100(5)	
STOP		J100(4)	
+ 5 V Signature - 00UP			
I/O Decoding		Processor Address Bus	
U504(7)	9COH	U501(3)	0000
U504(9)	5108	U501(5)	H42C
U504(10)	6A18	U501(7)	000U
U504(11)	HU98	U501(9)	0055
U504(12)	1U5P	U501(12)	0033
U504(13)	U4UC	U501(14)	UUUU
U504(14)	HFA1	U501(16)	4074
U504(15)	488H	U501(18)	0000

**Table 7-34 Processor Data Bus and RAM Address Bus Signatures**

<b>Signature Analyzer Setup</b>			
<b>Signal</b>	<b>Polarity</b>	<b>Connection</b>	
CLOCK		TP500 " $\overline{\text{FPS}}$ "	
START		U10 (12) or CR1 (Cathode of Green LED)	
STOP		U10 (12) or CR1 (Cathode of Green LED)	
+ 5 V Signature - 5UAH			
<b>Processor Data Bus</b>			
U105(2)	AHC7	U102(2)	U549
U105(3)	UPA8	U102(3)	7P9A
U105(4)	U81U	U102(4)	750U
U104(5)	6F50	U102(5)	C11U
U105(6)	33PP	U102(6)	9FH6
U105(7)	2887	U102(7)	F8AP
U105(8)	4949	U102(8)	H51A
U105(9)	P6F9	U102(9)	5PU4
<b>Signature Analyzer Setup</b>			
<b>Signal</b>	<b>Polarity</b>	<b>Connection</b>	
CLOCK		A40TP406 " $\overline{\text{PBG}}$ "	
START		J100(5)	
STOP		J100(4)	
<b>NOTE</b>			
<i>These signatures require an A30 Assembly with a properly operating RAM bus arbitrator installed in the -hp-3561A.</i>			
+ 5 V Signature - 5UAH			
<b>RAM Address Bus</b>			
U705(3)	U92U	U706(3)	C8F3
U705(5)	H5CC	U706(5)	7P99
U705(7)	C78P	U706(7)	00U3
U705(9)	H18F	U706(9)	79U0
U705(12)	34H8	U706(12)	P4CA
U705(14)	P931	U706(14)	A516
U705(16)	79H7	U706(16)	5CH6
U705(18)	5U94	U706(18)	7A88

Table 7-35 A40 Assembly Signal Connections

## INPUTS

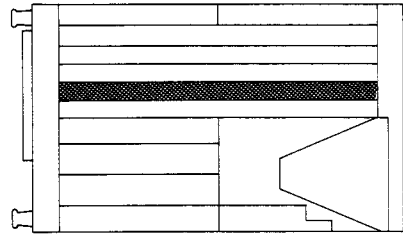
Signal Name	Functional Block	Connector Number	Origin Assembly
<u>BUBI</u>	A	P41(A5)	A65
<u>DMAI</u>	A	P41(A7)	A20
<u>DSPH</u>	J	P41(B5)	A60
<u>FFTI</u>	A	P41(A8)	A30
<u>HPCI</u>	A	P41(B7)	A50
<u>HPDI</u>	A	P41(B6)	A50
<u>LOW + 5</u>	Q	P42(B13)	A70
<u>PBC</u>	I	P42(B16)	A30
<u>PWR FAIL</u>	A	P41(B4)	A71
<u>SINT</u>	A	P41(B12)	A50

## OUTPUTS

Signal Name	Functional Block	Connector Number	Destination Assembly
<u>BUBS</u>	M	P41(A10)	A65
<u>CMOSS</u>	M	P41(B10)	A65
<u>DSPS</u>	M	P41(A9)	A60
<u>FPS</u>	M	P41(B8)	A81
<u>HPIBS</u>	M	P41(B11)	A50
<u>LOS</u>	M	P41(A11)	A50
<u>PBLDS</u>	L	P41(A12)	A30
<u>PBR</u>	I	P42(A16)	A30
<u>PBUDS</u>	L	P41(A13)	A30, A50
<u>PRAMRE</u>	I	P41(A4)	A30
<u>PRIOS</u>	I	P42(B17)	A30
<u>RESET</u>	Q	P41(B3)	A20, A30, A50, A60, A66/65, A81
100 kHz	S	P41(A3)	A30
4 MHz	R	P41(B2)	A50, A66/65
20.48 MHz	V	P41(A2)	A15, A20, A30

## I/O SIGNALS

Signal Name	Functional Block	Connector Number	Destination Assembly
Processor Address Bus PAB0 - PAB5	L	P41(A14 - A16) P41(B14 - B16)	A50, A60, A66/65
Processor Data Bus PDB0 - PDBF	G	P41(A17 - A24) P41(B17 - B24)	A30, A50, A60, A65/66
RAM Address Bus RAB0 - RABF	B	P42(A4 - A11) P42(B4 - B11)	A20, A30



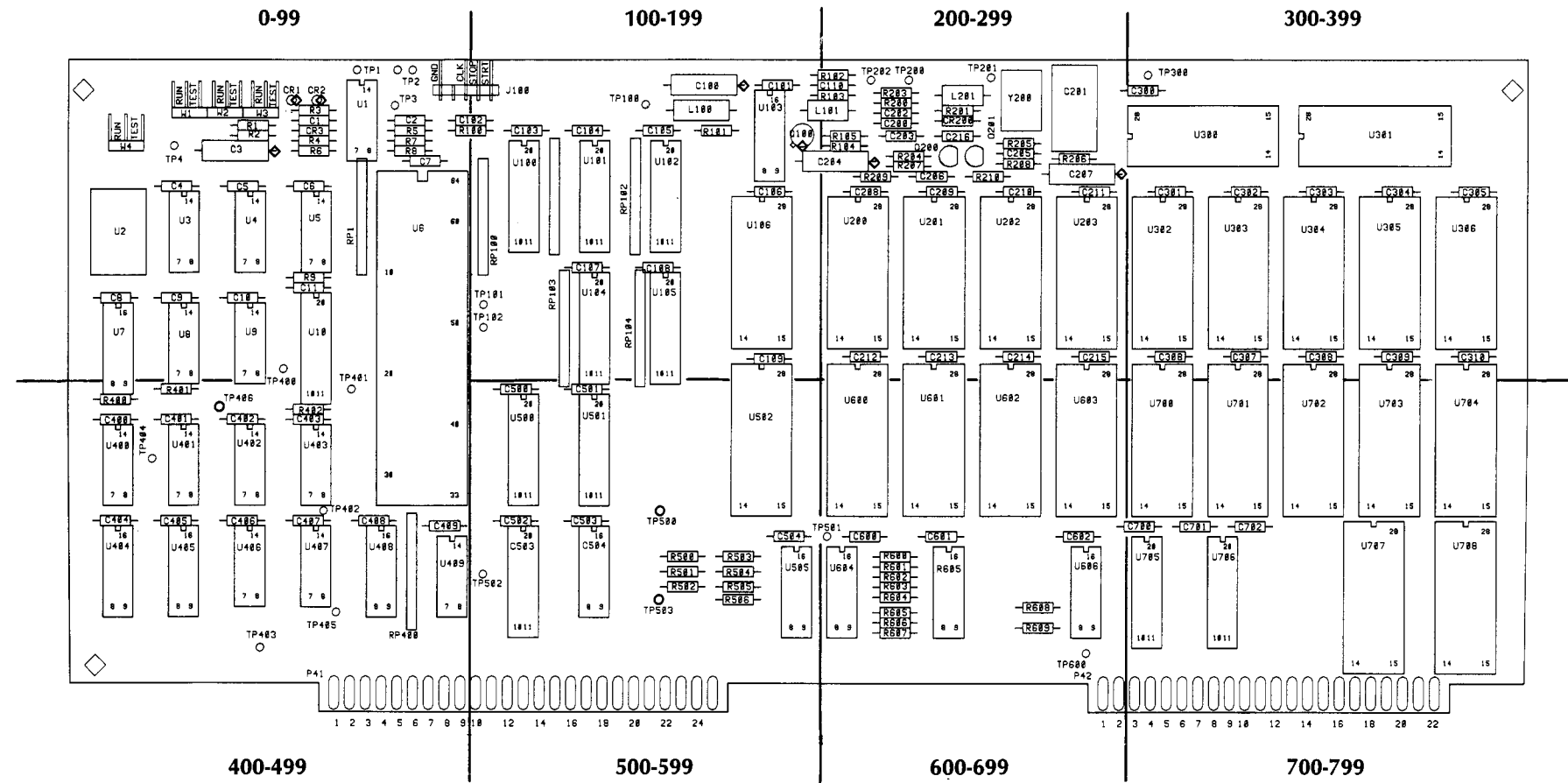
A40 Assembly  
Test Jumpers  
W1, W2, W3, and W4



Test Position



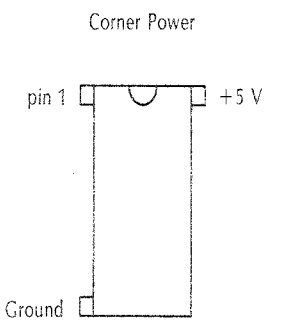
Run Position



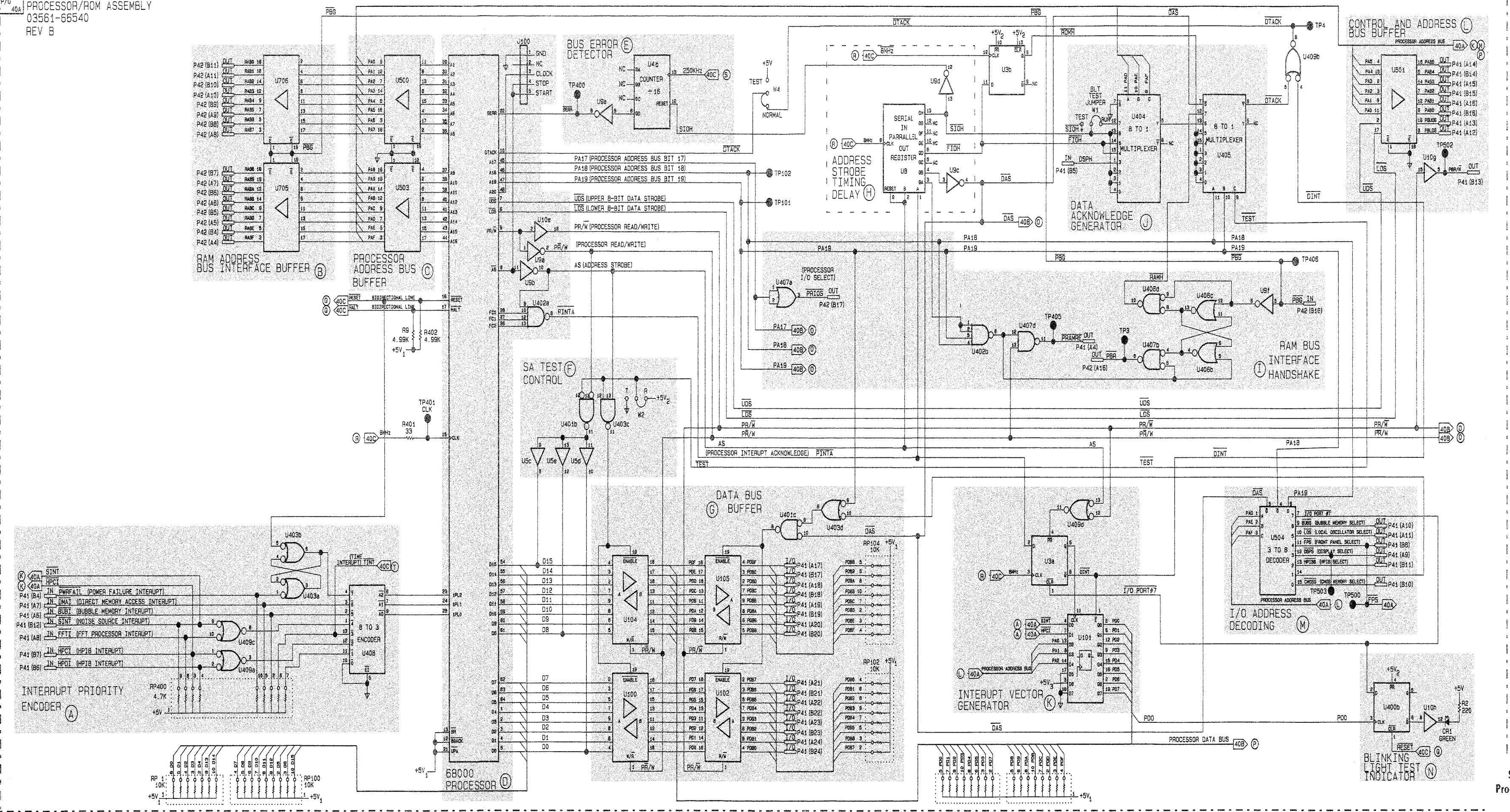


A40 Assembly

All integrated circuits are corner powered except those shown in the table below. Corner powered ICs have ground connected to the lower left pin, and +5 V connected to the upper right pin regardless of the total pin count. (eg., for a 16 pin DIP, ground is connected to pin 8 and +5 V is connected to pin 16)

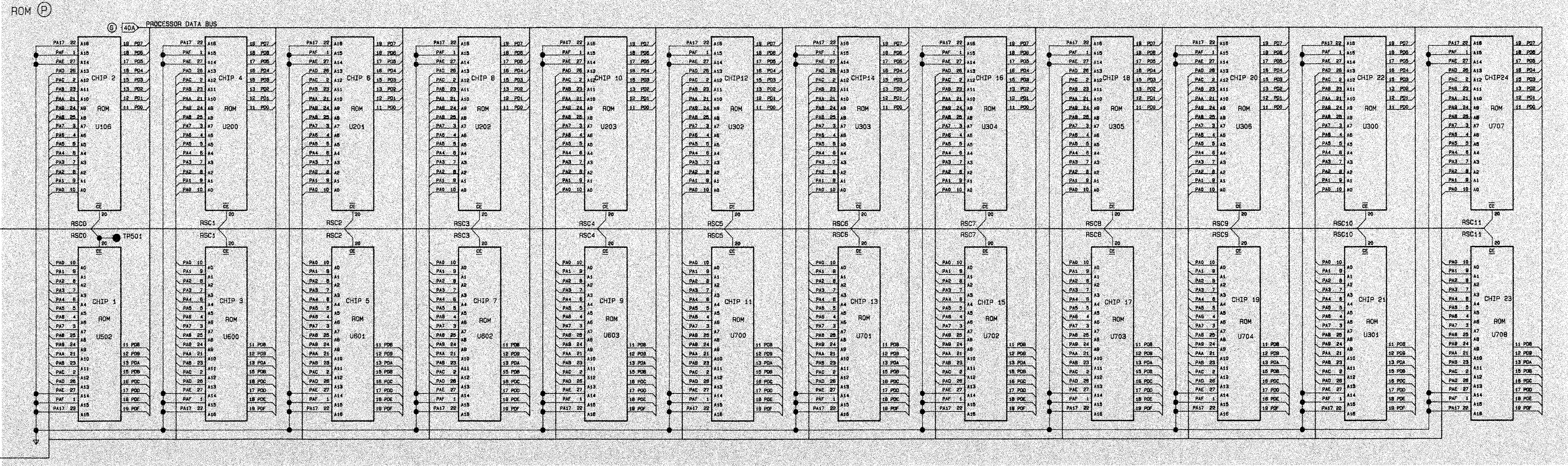
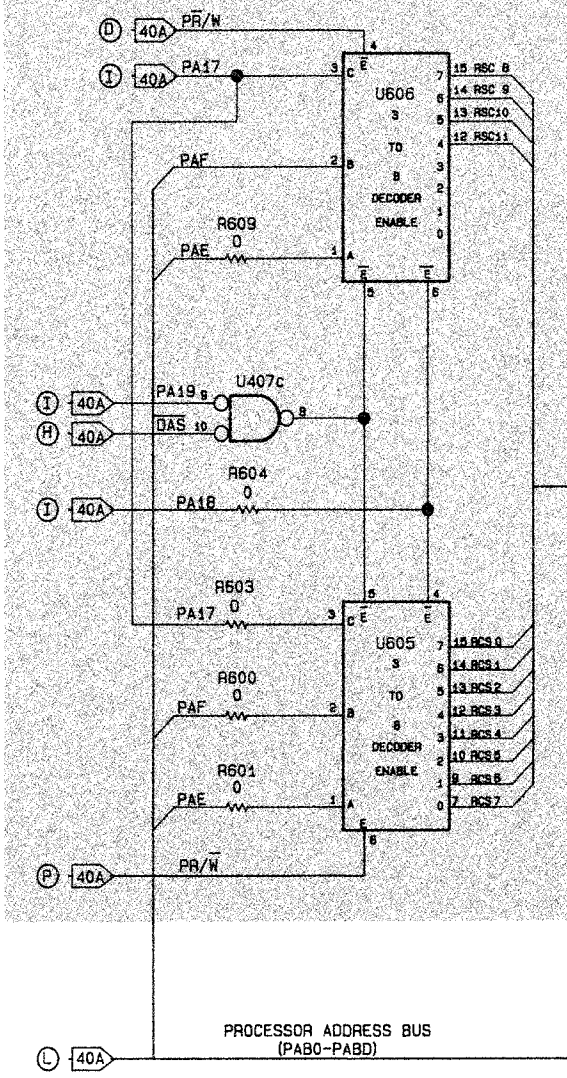


	+5V1	+5V4	GND
U1		5	12
U6	14,49	16,53	
U103		16	7

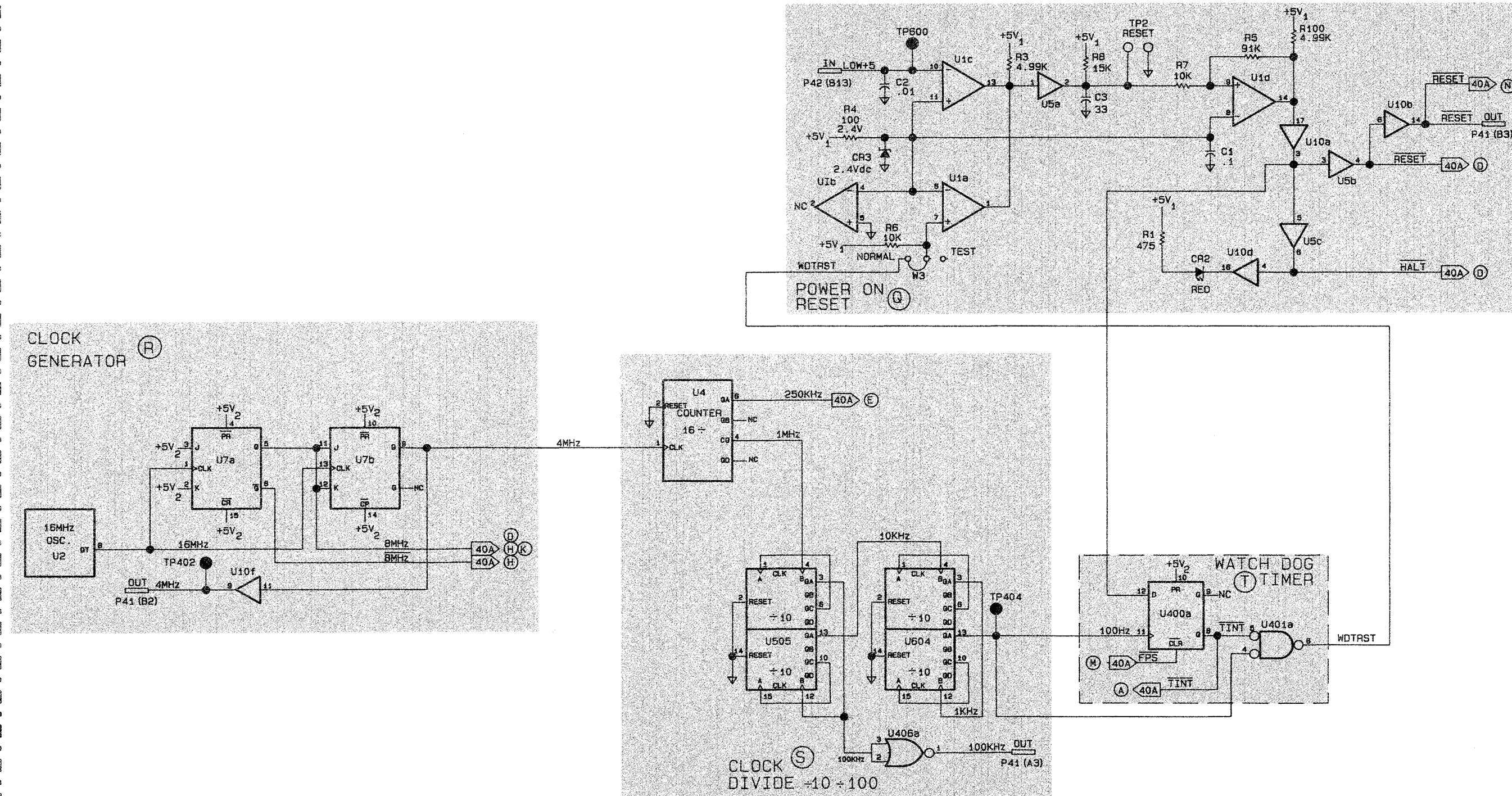


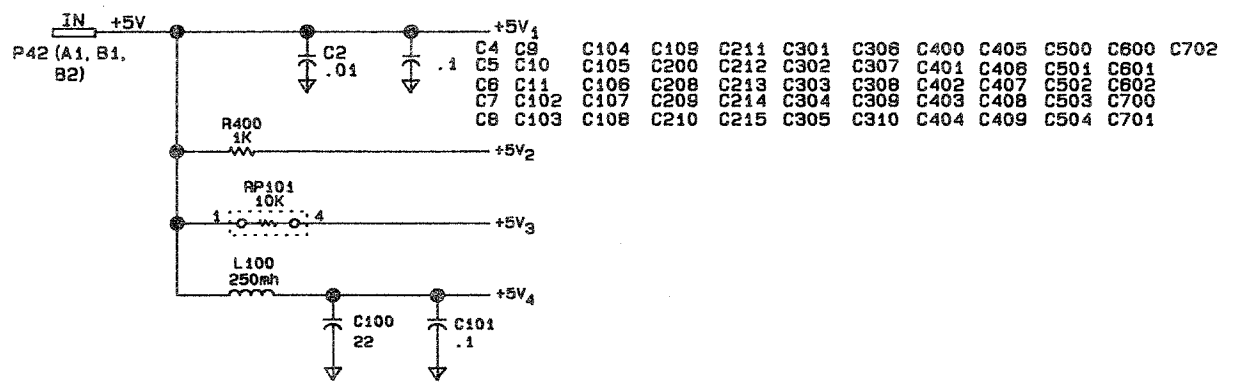
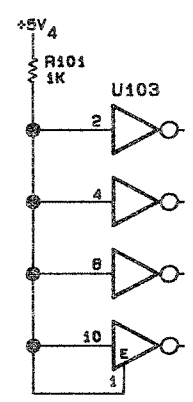
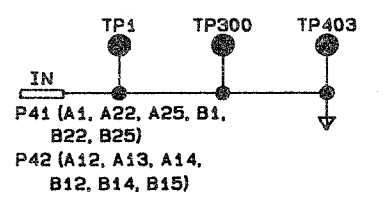
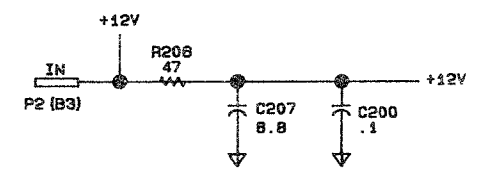
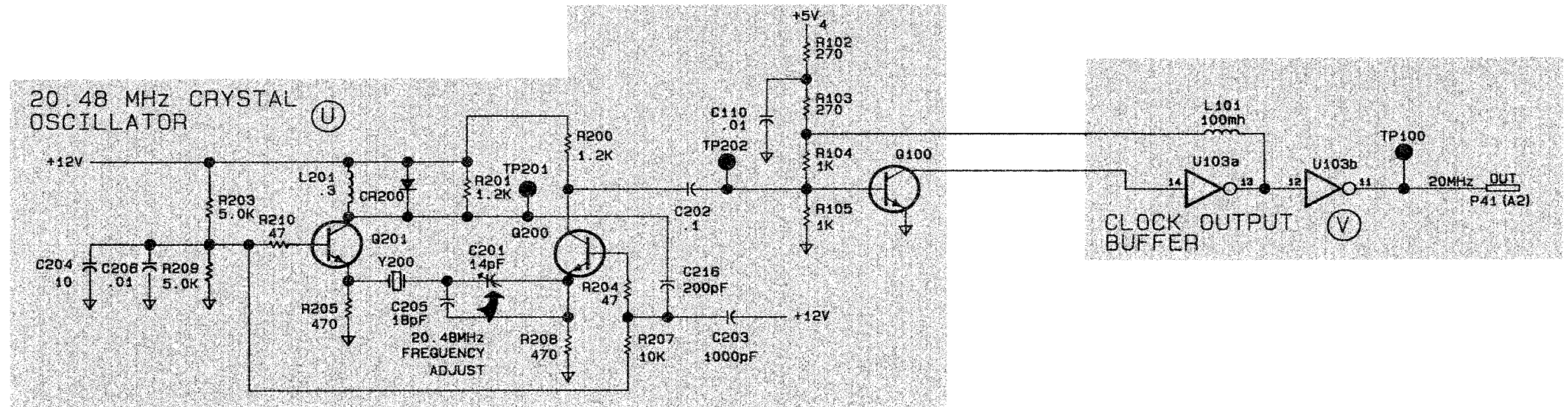


ROM ADDRESSING  
DECODING









## **7-19 A50 LOCAL OSCILLATOR/NOISE SOURCE ASSEMBLY**

### **7-20 Local Oscillator/Noise Source Circuit Description**

#### **GENERAL**

The A50 Assembly contains three separate operational circuits. They are: Local Oscillator, Noise Source and HP-IB. These circuits are described in general in the following three paragraphs and in detail after that.

The Local Oscillator is used when measuring in the zoom mode. It is set to the center frequency value of the zoom measurement and mixed with the incoming signal. The generated result is then FFTed and displayed. It is also used to shift the frequency band of the noise source so the resulting frequency content of the noise will track that of the measurement span.

The Noise Source generates random, periodic random and impulse signals which are band limited as determined by the frequency span of the measurement. The output is connected to the rear panel SOURCE BNC.

The HP-IB circuitry uses an Integrated Circuit to interface the -hp-3561A with the IEEE-488-1978 interface bus.

The theory that follows describes the functional blocks of each of the three previously mentioned operational circuits. Table 7-36 identifies and describes the signals used on this assembly.

#### **[A] PHASE LATCH**

The Phase Latch loads and stores the desired Local Oscillator frequency from the processor data bus. The data is actually a phase increment where 360 degrees equals 256kHz.

#### **[B] PHASE CORRECTION**

The Phase Correction contains the phase information of the local oscillator signal. This information is read by the processor so it can determine the phase of the input signal being measured.

**[C] PHASE INCREMENT ADDER**

This circuit adds the phase increment with the prior phase to calculate the new current phase with the increment ROM. The increment ROM performs a modulus 125 conversion of the lower 7 bits of the phase.

**[D] ANGLE ACCUMULATOR**

The Angle Accumulator latches the current phase angle which is fed back to the input of the Phase Increment Adder [C], to the Interpolator [J] and to the Sine Table [G].

**[E] TIMING STATE MACHINE**

The Timing State Machine generates the clock signals which control the timing of the A50 Assembly.

**[F] QUADRANT SHIFTER**

The Quadrant Shifter keeps track of which of the four quadrants (90 degrees each) the Local Oscillator is in. The states of AP18 and AP19 determine which quadrant and LOSM1 determines Sine or Cosine.

**[G] SINE TABLE**

These two ROMs contain both the 15 bit Sine/Cosine values for angles at increments of about 0.09 degrees, and the 8 bit slope numbers which allow the Local Oscillator to compute values for in-between angles. U507 contains the LSB bits for the sine values and U506 contains the MSB bits for the sine values along with the 8 bit slope numbers.

**[H] SLOPE DATA REGISTER**

This circuit is a parallel-in serial-out register which loads the Slope information from the Sine Table circuit and shifts it out serially to the Interpolator [J].

**[I] SINE DATA REGISTER**

This is a parallel-in serial-out circuit which loads in the sine data from the sine table and shifts it out to the Interpolator [J].

**[J] INTERPOLATOR**

The Interpolator circuit takes the slope information and the quadrant information and calculates the sine values for the 250 points between the sine points stored in the sine table ROMs. The interpolated result is output to the Local Oscillator Output [L].

**[K] GCLOCK GENERATOR**

The GCLOCK signal is the main A50 Assembly clock. In normal operation, it runs at 10.24 MHz. When the -hp-3561A operates in External Sample Rate, GCLOCK becomes a pulse train of 40 pulses, each train comprising one complete Local Oscillator cycle. Each train is started by a rising edge of SYNC2. SYNC2 may not exceed 256kHz.

**[L] LOCAL OSCILLATOR OUTPUT**

The Local Oscillator Output circuit has three data outputs: +COSINE, -SINE and Local Oscillator Output. The +COSINE and -SINE are used to set the center frequency of a zoom measurement. The Local Oscillator Output is used to shift the frequency band of the Noise Source such that the noise source frequency content falls within the bandwidth of the zoom measurement.

**[M] I/O CONTROL PORT**

This circuit latches processor data bits 0 through 7 which are then used by the A50 Assembly as control signals.

**[N] CLOCK****[O] SERIAL FEEDBACK REGISTERS****[P] NOISE SOURCE ROM ADDRESS REGISTERS**

In random mode, the Serial Feedback Registers and the Noise Source Address Registers form a 36 bit shift register. Input bits are generated by Exclusive ORing bits 13 and 33 and inverting the result. In effect, the circuit is a digital tapped delay line.

In Pseudo-random and Impulse modes, the Noise Source ROM Address Registers form a 12 bit counter which steps through the 4096 baseband or 2048 zoom points.

**[Q] RANDOM NOISE ROM**  
**[R] PERIODIC NOISE ROM**

ROM U700 takes the fourteen address bits and filters them by doing a weighted sum. Bits 6 and 7 weigh most heavily, bits 0 and 13 are weighted the least. U700 contains the sequences for a random signal. U701 contains the sequences for periodic random and impulse signals but does not act as a filter.

**[T] CLOCK SYNCHRONIZING LATCH**

This circuit latches the data from the noise ROMs and at the correct time, shifts the data out to the mixer circuitry.

**[W] LOCAL OSCILLATOR/NOISE SOURCE MIXER**  
**[X] LOCAL OSCILLATOR INTERFACE**

U201 takes the parallel Local Oscillator data and shifts it out serially to U704 where it is multiplied by the noise data. In Zoom, the Local Oscillator data shifts the frequency spectrum of the noise data so it is centered around the measurement's center frequency.

**[AA] SERIAL TO PARALLEL CONVERTER**  
**[CC] D TO A CONVERTER**  
**[FF] PROGRAMMABLE LOG ATTENUATOR**

The noise data is converted from serial to parallel by U306 and latched by U307. The digital parallel output is then converted to an analog signal by U402 and buffered by U403. The analog output is then fed to a log programmable attenuator U400.



**Table 7-36 A50 Assembly Signal Descriptions**

<b>Signal</b>	<b>Description</b>
BBS	BaseBand Sync: Indicates the end of a baseband record.
$\overline{\text{BB}}/\text{ZOOM}$	$\overline{\text{BaseBand}}/\text{ZOOM}$ : Signal from the processor used to setup the A50 Assembly for Baseband or Zoom measurements.
CSR1 THROUGH CSR4	Chip Select Read 1 through 4: Processor Address signals used to enable various ports to output their data.
CSW1 THROUGH CSW4	Chip Select Write 1 through 4: Processor Address signals used to enable various ports to input data.
ESR*4	Effective Sample Rate multiplied by 4: Used by the A50 Assembly as a clock. The effective sample rate is the ADC sample rate clock.
GCLOCK	Gated CLOCK: This is the main processing clock for the A50 Assembly. It is a 40 pulse clock train running at 256kHz.
$\overline{\text{LOS}}$	Local Oscillator Select: Processor Address signal used to access the A50 Assembly input and output ports.
LOSM1 THROUGH LSOMB	Local Oscillator State Machine 1 through 8: 8 Clocks generated by the A50 State Machine which provide the timing for the A50 Assembly.
NB0 THROUGH NB7	Noise Bit 0 through 7: 8 Data bits output by the two noise ROMs.
$\overline{\text{PER}}/\text{IMP}$	$\overline{\text{PERiodic}}/\text{IMPulse}$ : Processor setup signal used in conjunction with the RANDOM signal to enable either the periodic or the impulse noise output.
RANDOM	RANDOM: Processor setup signal used to enable the A50 Assembly to be in the random or periodic/impulse mode of operation.
SBO THROUGH SBD	Source Bits 0 through D: 14 Address bits which are generated by the ROM Address Counter circuit and are used to address the data locations within the Noise ROMs U700 and U701.
SYNC2	SYNC2: Sample rate clock from the A20 Assembly. A rising edge triggers one cycle of the Local Oscillator. When cycled, the A50 Assembly outputs one complex value to the Digital Filters and one real value to the source.
TRIG0 TRIG1	TRIGger0 and TRIGger2: Processor signals which determine which trigger source the -hp-3561A will use. This circuit function runs independently of the rest of the A50 Assembly.
ZPH TRIGGER	Zoom PHase TRIGGER: Processor signal used to latch information into the phase correction latches.
ZS	Zoom Sync: Used in the Zoom mode to indicate the end of a record. This signal has the same function the BBS signal has in Baseband measurements.

## 7-21 Troubleshooting The Local Oscillator/Noise Source

### GENERAL

Although there are only three major operational circuits, there are eight separate subcircuits. The troubleshooting procedure will be to verify proper operation of particular subcircuits, one at a time, in order of dependency. Table 7-37 lists the order of dependency. In this table, level one circuits must be operational before level two circuits can be checked, etcetera. Test Routines 150, 151, 152, 153 and 154 will be used to troubleshoot this assembly. Troubleshooting consists of verifying waveforms with an oscilloscope and Digital Signature Analysis. Also, some user-programmable parameters entered via the front panel keys are used to preset circuit conditions.

**Table 7-37 A50 Circuit Troubleshooting Order**

Level	Functional Blocks
1	Processor Address Decoding: S
2	I/O Control Port: M
3	GCLOCK Generator: K
4	Timing State Machine: E
5	Local Oscillator Circuitry: A, B, C, D, E, F, G, H, I, J, K, L
6	Local Oscillator Interface: X
7	Noise Source Circuitry: N, O, P, Q, R, T, U, V, W, Y, Z, AA, BB, CC, EE, FF, HH, II
8	HP-IB I/O Circuitry: DD, GG

### [S] PROCESSOR ADDRESS DECODING

Troubleshoot this circuit using the Signature Analyzer as a logic probe. The procedure will be to monitor the pins of U501 while running or starting and stopping the diagnostic test.

1. Program the -hp-3561A in Test Routine 150 by pressing the following front panel keys:  
  
MODE ..... TEST SELECT ..... 150 ENTER
2. Initiate continuous testing by pressing the START CONT TST softkey.
3. Use the logic probe and verify that U501(12,13,14,15) are toggling. If they are not, replace U501.
4. Stop the test by pressing the softkey STOP TEST.
5. Place the logic probe on U501(10, 11) one at a time and press the soft key START SNGL TST. These pins should pulse low when the test routine is initiated. If they do not, replace U501.

**[M] I/O CONTROL PORT**

Troubleshoot this circuit using the Signature Analyzer as a logic probe. The procedure will be to monitor U602(6,9,12,16) while initiating particular measurement parameters.

1. Press the front panel PRESET key.
2. Press the front panel TRIG SEL key to display the trigger selection menu on the CRT.
3. Use the logic probe to verify that U602(6,9) are low.
4. Press the softkey FREE RUN/TRIGGER so TRIGGER is highlighted.
5. Probe U602(6,9) and press the softkey EXTERNAL TRIGGER and verify that they go high. Press the softkey INTERNAL TRIGGER and verify that they go low. If not, replace U602.
6. Press the front panel PRESET key.
7. Press the front panel SOURCE key to display the source selection menu on the CRT.
8. Use the logic probe to verify that U602(12) is high and U602(16) is low.
9. Probe U602(12,16) and press the softkey IMPULSE and verify that they change state. Pin 12 should go low and pin 16 should go high. If not, replace U602.

**[K] GCLOCK GENERATOR**

Troubleshoot this circuit by using the Signature Analyzer as a logic probe. The procedure will be to monitor the pins of U500 and U505 for a toggling condition with the -hp-3561A running in the PRESET state.

1. Press the front panel PRESET key.
2. Use the logic probe and verify that U500(1,3,6) and U505(1,6,9,11) are toggling.
3. If U500(1) is not toggling, check U807(1) for a toggling condition. If it is not toggling, there may be a failure in the Timing State Machine. Troubleshoot that circuit.
4. If any of the pins are not toggling, replace the suspected IC.

**[E] TIMING STATE MACHINE**

Troubleshoot this circuit by using the Signature Analyzer as a logic probe. The procedure will be to monitor the pins of U606 for a toggling condition while the -hp-3561A is operating in the PRESET state.

1. Press the front panel PRESET key.
2. Use the logic probe and verify that U606(6,7,8,9 and 12 through 19) are toggling.
3. If any are not, replace the suspected IC. Also note that the outputs of U606 (LOSM1 through LOSM8) clock other functional circuits which may be holding these output lines low or high.

**LOCAL OSCILLATOR CIRCUITRY**

Troubleshooting this circuitry consists of verifying signatures with a Signature Analyzer while running a diagnostic test routine. The Local Oscillator Functional Circuits are listed below along with the table which contains their correct signatures.




[A] Phase Latch	Table 7-38
[B] Phase Correction	Table 7-38
[C] Phase Increment Adder	Table 7-38
[D] Angle Accumulator	Table 7-38
[F] Quadrant Shifter	Table 7-38
[G] Sine Table	Table 7-39
[H] Slope Data Register	Table 7-40
[I] Sine Data Register	Table 7-40
[J] Interpolator	Table 7-40
[L] Local Oscillator Output	Table 7-40

1. Program the -hp-3561A into Test Routine 150 by pressing the following front panel keys:

MODE ..... TEST SELECT.....150 ENTER

2. Initiate continuous testing by pressing the START CONT TST softkey.
3. Check the signatures given in Table 7-38 to troubleshoot those functional circuits listed.
4. Check the signatures given in Table 7-39 to troubleshoot the Sine Table ROMs. Note that there are two setups for the Signature Analyzer Clock. Both setups must be checked.
5. Check the signatures given in Table 7-40 to troubleshoot those functional circuits listed.

**Table 7-38 Local Oscillator Signatures For Functional Circuits [A], [C], [D] And [F]**

Signature Analyzer Setup			
Signal	Polarity	Connection	
Clock		A50 J1 "LOSM1"	
Start		A50 J100 "STRT"	
Stop		A50 J100 "STOP"	
+ 5 V Signature - 5C1C			
[A] Phase Latch Circuit		[C] Phase Increment Adder Circuit	
U504(2)	8UA8	U6(1)	15F1
U504(5)	6P45	U6(4)	H2A1
U504(6)	9231	U6(10)	HFUC
U504(9)	F7H4	U6(13)	1FP8
U504(12)	41C4		
U504(15)	CU8P	U8(1)	486U
U504(16)	157F	U8(4)	U914
U504(19)	564F	U8(10)	4949
		U8(13)	7098
U600(2)	46U9		
U600(5)	5H83	U9(1)	40AP
U600(6)	CF6P	U9(4)	5A19
U600(9)	U0AC	U9(10)	4894
U600(12)	A54P	U9(13)	7177
U600(15)	232P		
U600(16)	HH14	U106(1)	FFU2
U600(19)	77P6	U106(4)	84AP
		U106(10)	HOFP
		U106(13)	C804
U601(2)	2951		
U601(5)	8ACP	U107(1)	UC4H
U601(6)	2C26	U107(4)	3PHC
U601(9)	5C1C	U107(10)	00F9
U601(12)	5C1C (HIGH)	U107(13)	199C




**Table 7-38 Local Oscillator Signatures for Functional Circuits [A], [C], [D] and [F] (Cont'd)**

[D] Angle Accumulator Circuit		[F] Quadrant Shifter Circuit	
U1(2)	384F	U5(1)	3C12
U1(5)	24A4	U5(4)	H56U
U1(7)	6950	U5(10)	5C1C
U1(10)	8AP0	U5(13)	7F80
U1(12)	8P74		
U1(15)	PP7H		
U102(2)	F257		
U102(5)	5A27		
U102(6)	F0UA		
U102(9)	U125		
U102(12)	C715		
U102(15)	F785		
U102(16)	HAA1		
U102(19)	AU52		
U105(2)	AH0F		
U105(5)	2057		
U105(7)	38CC		
U105(10)	A44A		
U105(12)	UF8A		
U105(15)	A437		

**Table 7-39 Local Oscillator Signatures For Functional Circuit [G]**

There are two Signature Analyzer setups necessary to check the ROMs. Both setups are given along with the signatures. If there is a signature mismatch in either setup, replace the defective ROM.




**Signature Analyzer Setup #1**

Signal	Polarity	Connection
Clock		A50 J1 "LOSM6"
Start		A50 J100 "STRT"
Stop		A50 J100 "STOP"

+ 5 V Signature - 7576

U506(9)	4209	U507(9)	UPPC
U506(10)	111H	U507(10)	330P
U506(11)	2C70	U507(11)	34FA
U506(13)	C1AP	U507(13)	9CP5
U506(14)	45FH	U507(14)	UP0F
U506(15)	HC46	U507(15)	C525
U506(16)	H148	U507(16)	06U3
U506(17)	0000	U507(17)	3AU3



















**Signature Analyzer Setup #2**

Signal	Polarity	Connection
Clock		A50 J1 "LOSM6"
Start		A50 J100 "STRT"
Stop		A50 J100 "STOP"

+ 5 V Signature - 7576

U506(9)	C941	U507(9)	UPPC
U506(10)	3H95	U507(10)	330P
U506(11)	41HP	U507(11)	34FA
U506(13)	11U5	U507(13)	9CP5
U506(14)	H401	U507(14)	UP0F
U506(15)	05F7	U507(15)	C525
U506(16)	49P9	U507(16)	06U3
U506(17)	UH5A	U507(17)	3AU3

**Table 7-40 Local Oscillator Signatures For Functional Circuits [H], [I], [J] And [L]**

<p>There are two Signature Analyzer setups necessary to fully check functional circuit [J] Interpolator. The first setup is used to check all four functional circuits while the second setup is only used as a second check for functional circuit [J].</p> <p><b>Signature Analyzer Setup #1</b></p> <table border="1"> <thead> <tr> <th>Signal</th> <th>Polarity</th> <th>Connection</th> </tr> </thead> <tbody> <tr> <td>Clock</td> <td></td> <td>A50 J100 "CLK"</td> </tr> <tr> <td>Start</td> <td></td> <td>A50 J100 "STRT"</td> </tr> <tr> <td>Stop</td> <td></td> <td>A50 J100 "STOP"</td> </tr> </tbody> </table> <p>+5 V Signature - C21U</p>				Signal	Polarity	Connection	Clock		A50 J100 "CLK"	Start		A50 J100 "STRT"	Stop		A50 J100 "STOP"																				
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Start		A50 J100 "STRT"																																	
Stop		A50 J100 "STOP"																																	
<p>[H] Slope Data Register</p> <table border="1"> <tbody> <tr> <td>U7(2)</td> <td>UFAA</td> </tr> <tr> <td>U7(12)</td> <td>CUPA</td> </tr> </tbody> </table> <p>[I] Sine Data Register</p> <table border="1"> <tbody> <tr> <td>U502(13)</td> <td>C3F0</td> </tr> <tr> <td>U502(15)</td> <td>AUC8</td> </tr> </tbody> </table> <p>[J] Interpolator</p> <table border="1"> <tbody> <tr> <td>U101(6)</td> <td>3UAU</td> </tr> <tr> <td>U4(3)</td> <td>0460</td> </tr> <tr> <td>U4(10)</td> <td>0813</td> </tr> </tbody> </table>		U7(2)	UFAA	U7(12)	CUPA	U502(13)	C3F0	U502(15)	AUC8	U101(6)	3UAU	U4(3)	0460	U4(10)	0813	<p>[L] Local Oscillator Output</p> <table border="1"> <tbody> <tr> <td>U200(3)</td> <td>C97H</td> </tr> <tr> <td>U200(7)</td> <td>5220</td> </tr> <tr> <td>U200(8)</td> <td>1HAH</td> </tr> <tr> <td>U200(9)</td> <td>PO96</td> </tr> <tr> <td>U200(10)</td> <td>6P07</td> </tr> <tr> <td>U200(11)</td> <td>5P3U</td> </tr> <tr> <td>U200(13)</td> <td>717C</td> </tr> <tr> <td>U200(14)</td> <td>A75H</td> </tr> <tr> <td>U200(15)</td> <td>U8C3</td> </tr> </tbody> </table>		U200(3)	C97H	U200(7)	5220	U200(8)	1HAH	U200(9)	PO96	U200(10)	6P07	U200(11)	5P3U	U200(13)	717C	U200(14)	A75H	U200(15)	U8C3
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U200(14)	A75H																																		
U200(15)	U8C3																																		
<p>The following Signature Analyzer setup is for functional circuit [J] Interpolator only.</p> <p><b>Signature Analyzer Setup #2</b></p> <table border="1"> <thead> <tr> <th>Signal</th> <th>Polarity</th> <th>Connection</th> </tr> </thead> <tbody> <tr> <td>Clock</td> <td></td> <td>A50 J100 "CLK"</td> </tr> <tr> <td>Start</td> <td></td> <td>A50 J100 "STRT"</td> </tr> <tr> <td>Stop</td> <td></td> <td>A50 J100 "STOP"</td> </tr> </tbody> </table> <p>+5 V Signature - C21U</p>				Signal	Polarity	Connection	Clock		A50 J100 "CLK"	Start		A50 J100 "STRT"	Stop		A50 J100 "STOP"																				
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U3(2)	2F80																																		
U3(9)	49C5																																		



**[X] LOCAL OSCILLATOR INTERFACE**




Troubleshoot this circuit by verifying the signatures with a Signature Analyzer while running Diagnostic Test Routine 150.

1. Program the -hp-3561A into Test Routine 150 by pressing the following front panel keys:

MODE ..... TEST SELECT.....150 ENTER

2. Initiate the continuous testing by pressing the START CONT TST softkey.
3. Check the signatures given in Table 7-41 to troubleshoot Functional Circuit [X].

**Table 7-41 Local Oscillator Interface Signatures For Functional Circuit [X]**

Signature Analyzer Setup		
Signal	Polarity	Connection
Clock		A50 J100 "CLK"
Start		A50 J100 "STRT"
Stop		A50 J100 "STOP"
+ 5 V Signature - C21U		
[X] Local Oscillator Interface		
U201(12)	6P58	
U302(8)	5220	
U302(11)	0000	

**NOISE SOURCE CIRCUITRY**

There are two techniques used to troubleshoot the Noise Source circuitry. The first is to use an oscilloscope to check analog waveforms while running Diagnostic Test Routine 151. This Test Routine programs the Noise Source to output a 250 Hz Sinewave and is used to troubleshoot the analog portion of the Noise Source circuitry. The second technique is to use a Signature Analyzer to verify the proper operation of the digital portion of the Noise Source. Test Routines 150, 152 and 153 are used for Signature Analysis troubleshooting.

The Noise Source Functional Circuits are listed below in the order in which they should be checked. Also listed is the table or figure which contains their correct signatures or waveforms.

Note that the troubleshooting order does not match the table order. Instead, the tables are organized as determined by the Signature Analyzer Setup.

[O] Serial Feedback Registers	Table 7-42
[P] Noise Source ROM Address Counters	Table 7-42
[Q] Random Noise ROM	Table 7-43
[R] Periodic Noise ROM	Table 7-42
[T] Clock Synchronizing Latch	Table 7-42
[W] Local Oscillator/Noise Source Mixer	Table 7-44
[AA] Serial To Parallel Data Converter	Table 7-44
[CC] D/A Converter	Figure 7-29
[FF] Programmable Log Attenuator	Figure 7-30
[HH] 100kHz Lowpass	Figure 7-31
[II] Output	Figure 7-32
[EE] Noise Source Sync Generator	Table 7-43
[Y] Trigger Select	Table 7-43










1. Program the -hp-3561A into the proper Test Routine, as determined by the table, by pressing the following front panel keys:

MODE ..... TEST SELECT .....xxx ENTER










Where xxx is the Test Routine Number (150, 151, 152 or 153).

2. Before checking signatures or waveforms, initiate continuous testing mode by pressing the START CONT TST softkey.
3. Check the signatures or the waveforms given in the appropriate table to troubleshoot the functional circuits indicated by that table.







**Table 7-42 Noise Source Signatures For Functional Circuits [O], [P], [R], And [T]**

<p>The following signatures are valid with the -hp-3561A running Diagnostic Test Routine 152.</p> <p><b>Signature Analyzer Setup</b></p> <table border="1"> <thead> <tr> <th>Signal</th> <th>Polarity</th> <th>Connection</th> </tr> </thead> <tbody> <tr> <td>Clock</td> <td></td> <td>A50 J200 "CLK"</td> </tr> <tr> <td>Start</td> <td></td> <td>A50 J100 "STRT"</td> </tr> <tr> <td>Stop</td> <td></td> <td>A50 J100 "STOP"</td> </tr> </tbody> </table> <p>+ 5 V Signature - 5C1C</p>			Signal	Polarity	Connection	Clock		A50 J200 "CLK"	Start		A50 J100 "STRT"	Stop		A50 J100 "STOP"																																																																						
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<p>[O] Serial Feedback Register</p> <table border="1"> <tbody> <tr> <td>U100(7)</td> <td>36U6</td> </tr> <tr> <td>U202(3)</td> <td>PH8H</td> </tr> <tr> <td>U202(4)</td> <td>U6F6</td> </tr> <tr> <td>U202(13)</td> <td>4C81</td> </tr> <tr> <td>U203(13)</td> <td>FFFC</td> </tr> <tr> <td>U300(10)</td> <td>F3UU</td> </tr> <tr> <td>U302(6)</td> <td>2P72</td> </tr> <tr> <td>U801(4)</td> <td>6HPP</td> </tr> </tbody> </table> <p>[R] Periodic Noise ROM</p> <table border="1"> <tbody> <tr> <td>U701(11)</td> <td>26FP</td> </tr> <tr> <td>U701(12)</td> <td>U1U8</td> </tr> <tr> <td>U701(13)</td> <td>HP35</td> </tr> <tr> <td>U701(15)</td> <td>8U6H</td> </tr> <tr> <td>U701(16)</td> <td>P180</td> </tr> <tr> <td>U701(17)</td> <td>A49P</td> </tr> <tr> <td>U701(18)</td> <td>4CC3</td> </tr> <tr> <td>U701(19)</td> <td>F270</td> </tr> </tbody> </table>		U100(7)	36U6	U202(3)	PH8H	U202(4)	U6F6	U202(13)	4C81	U203(13)	FFFC	U300(10)	F3UU	U302(6)	2P72	U801(4)	6HPP	U701(11)	26FP	U701(12)	U1U8	U701(13)	HP35	U701(15)	8U6H	U701(16)	P180	U701(17)	A49P	U701(18)	4CC3	U701(19)	F270	<p>[P] Noise Source ROM Address Counters</p> <table border="1"> <tbody> <tr> <td>U204(11)</td> <td>1C7C</td> </tr> <tr> <td>U204(12)</td> <td>36U6</td> </tr> <tr> <td>U204(13)</td> <td>6HPP</td> </tr> <tr> <td>U204(14)</td> <td>36U6</td> </tr> <tr> <td>U204(15)</td> <td>0000 (LOW)</td> </tr> <tr> <td>U205(11)</td> <td>C1C7</td> </tr> <tr> <td>U205(12)</td> <td>636U</td> </tr> <tr> <td>U205(13)</td> <td>F6HP</td> </tr> <tr> <td>U205(14)</td> <td>8HCH</td> </tr> <tr> <td>U205(15)</td> <td>0000 (LOW)</td> </tr> <tr> <td>U206(11)</td> <td>HC1C</td> </tr> <tr> <td>U206(12)</td> <td>C636</td> </tr> <tr> <td>U206(13)</td> <td>6F6H</td> </tr> <tr> <td>U206(14)</td> <td>H8HC</td> </tr> <tr> <td>U206(15)</td> <td>0000 (LOW)</td> </tr> </tbody> </table> <p>[T] Clock Synchronizing Latch</p> <table border="1"> <tbody> <tr> <td>U702(2)</td> <td>97AP</td> </tr> <tr> <td>U702(5)</td> <td>A5H9</td> </tr> <tr> <td>U702(6)</td> <td>A4H9</td> </tr> <tr> <td>U702(9)</td> <td>U0F0</td> </tr> <tr> <td>U702(12)</td> <td>47C6</td> </tr> <tr> <td>U702(15)</td> <td>998F</td> </tr> <tr> <td>U702(16)</td> <td>78UF</td> </tr> <tr> <td>U702(19)</td> <td>65U1</td> </tr> <tr> <td>U806(11)</td> <td>0000 (LOW)</td> </tr> <tr> <td>U807(8)</td> <td>5C1C (HIGH)</td> </tr> </tbody> </table>	U204(11)	1C7C	U204(12)	36U6	U204(13)	6HPP	U204(14)	36U6	U204(15)	0000 (LOW)	U205(11)	C1C7	U205(12)	636U	U205(13)	F6HP	U205(14)	8HCH	U205(15)	0000 (LOW)	U206(11)	HC1C	U206(12)	C636	U206(13)	6F6H	U206(14)	H8HC	U206(15)	0000 (LOW)	U702(2)	97AP	U702(5)	A5H9	U702(6)	A4H9	U702(9)	U0F0	U702(12)	47C6	U702(15)	998F	U702(16)	78UF	U702(19)	65U1	U806(11)	0000 (LOW)	U807(8)	5C1C (HIGH)
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U204(12)	36U6																																																																																			
U204(13)	6HPP																																																																																			
U204(14)	36U6																																																																																			
U204(15)	0000 (LOW)																																																																																			
U205(11)	C1C7																																																																																			
U205(12)	636U																																																																																			
U205(13)	F6HP																																																																																			
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U206(15)	0000 (LOW)																																																																																			
U702(2)	97AP																																																																																			
U702(5)	A5H9																																																																																			
U702(6)	A4H9																																																																																			
U702(9)	U0F0																																																																																			
U702(12)	47C6																																																																																			
U702(15)	998F																																																																																			
U702(16)	78UF																																																																																			
U702(19)	65U1																																																																																			
U806(11)	0000 (LOW)																																																																																			
U807(8)	5C1C (HIGH)																																																																																			

**Table 7-43 Noise Source Signatures For Functional Circuits [Q], [Y] And [EE]**

<p>The following signatures are valid with the -hp-3561A running in Test Routine 153.</p> <p><b>Signature Analyzer Setup</b></p> <table border="1"> <thead> <tr> <th>Signal</th> <th>Polarity</th> <th>Connection</th> </tr> </thead> <tbody> <tr> <td>Clock</td> <td></td> <td>A50 J200 "CLK"</td> </tr> <tr> <td>Start</td> <td></td> <td>A50 J200 "STRT"</td> </tr> <tr> <td>Stop</td> <td></td> <td>A50 J200 "STOP"</td> </tr> </tbody> </table> <p>+ 5 V Signature - 7A70</p>			Signal	Polarity	Connection	Clock		A50 J200 "CLK"	Start		A50 J200 "STRT"	Stop		A50 J200 "STOP"													
Signal	Polarity	Connection																									
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Start		A50 J200 "STRT"																									
Stop		A50 J200 "STOP"																									
<p>[Q] Random Noise ROM</p> <table border="1"> <tbody> <tr><td>U700(11)</td><td>P103</td></tr> <tr><td>U700(12)</td><td>518P</td></tr> <tr><td>U700(13)</td><td>A3AP</td></tr> <tr><td>U700(15)</td><td>0402</td></tr> <tr><td>U700(16)</td><td>H977</td></tr> <tr><td>U700(17)</td><td>UUFP</td></tr> <tr><td>U700(18)</td><td>7979</td></tr> <tr><td>U700(19)</td><td>H918</td></tr> </tbody> </table>	U700(11)	P103	U700(12)	518P	U700(13)	A3AP	U700(15)	0402	U700(16)	H977	U700(17)	UUFP	U700(18)	7979	U700(19)	H918	<p>[Y] Trigger Select</p> <table border="1"> <tbody> <tr><td>U808(7)</td><td>F748</td></tr> </tbody> </table> <p>[EE] Noise Source Sync Generator</p> <table border="1"> <tbody> <tr><td>U304(9)</td><td>F748</td></tr> <tr><td>U305(8)</td><td>99H4</td></tr> <tr><td>U500(8)</td><td>7A70 (HIGH)</td></tr> <tr><td>U803(6)</td><td>P3A4</td></tr> </tbody> </table>	U808(7)	F748	U304(9)	F748	U305(8)	99H4	U500(8)	7A70 (HIGH)	U803(6)	P3A4
U700(11)	P103																										
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U305(8)	99H4																										
U500(8)	7A70 (HIGH)																										
U803(6)	P3A4																										

**Table 7-44 Noise Source Signatures For Functional Circuits [W] And [AA]**

<p>The following signatures are valid with the -hp-3561A running Diagnostic Test Routine 150. Note there are two Signature Analyzer setups for checking Functional Circuit [AA].</p>			
<p><b>Signature Analyzer Setup #1</b></p>			
<b>Signal</b>	<b>Polarity</b>	<b>Connection</b>	
Clock		A50 J100 "CLK"	
Start		A50 J100 "STRT"	
Stop		A50 J100 "STOP"	
+ 5 V Signature - C21U			
[W] Local Oscillator/Noise Source Mixer			
U704(6)	0AFF		
[AA] Serial To Parallel Data Converter			
U306(3)	PP76		
U306(4)	1F2C		
U306(5)	P505		
U306(6)	1992		
U306(10)	P7H9		
U306(11)	18UF		
U306(12)	P76P		
U306(13)	18A7		
U806(6)	AH88		
<p><b>Signature Analyzer Setup #2</b></p>			
<b>Signal</b>	<b>Polarity</b>	<b>Connection</b>	
Clock		A50 J100 "CLK"	
Start		A50 J100 "STRT"	
Stop		A50 J100 "STOP"	
+ 5 V Signature - C21U			
[AA] Serial To Parallel Data Converter			
U307(2)	42UA	U307(12)	3PCP
U307(5)	C5P8	U307(15)	8P5P
U307(6)	FU52	U307(16)	0AA3
U307(9)	CU5A	U307(19)	4U63
U801(8)	C8H3		

**NOISE SOURCE TROUBLESHOOTING WAVEFORMS FOR FUNCTIONAL CIRCUITS [CC], [FF], [HH] AND [II].**

The following troubleshooting information is valid with the -hp-3561A running Diagnostic Test Routine 151.

**[CC] D/A CONVERTER**

Verify the waveform at TP DAC OUT with that shown in Figure 7-29. If the waveform is incorrect, use a Logic Probe to verify that U402(5,6,7,8,9,10,11,12) are toggling. If they are, replace U402 and U403 or the analog elements around them. If they are not, troubleshoot Functional Circuit [AA].

**[FF] PROGRAMMABLE LOG ATTENUATOR**

Verify the waveform at U401(6) with that shown in Figure 7-30. If the waveform is incorrect, use the logic probe to verify that U400(2,3,4,5,6,7) are all low. If they are not, replace U303. If they are, replace U400 and U401.

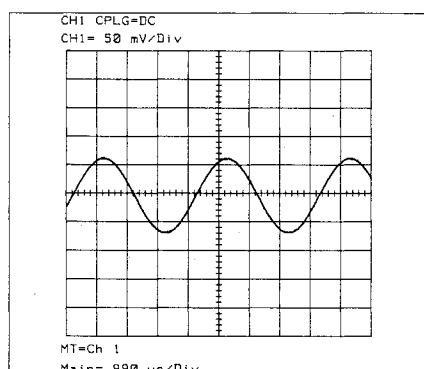
**[HH] 100kHz LOWPASS**

Verify the waveform at U404(6) with that shown in Figure 7-31. If the waveform is incorrect, troubleshoot this circuit.

**[II] OUTPUT**

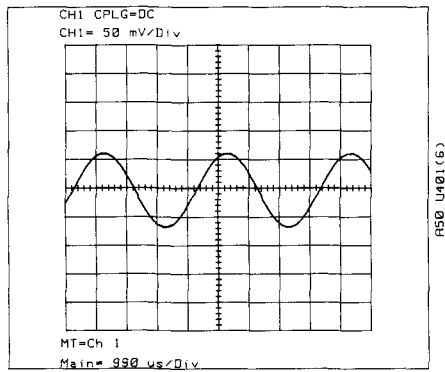
Verify the waveform at U901(4) with that shown in Figure 7-32. If the waveform is incorrect, troubleshoot this circuit.

**Figure 7-29 Correct Waveform At A50 TP DAC OUT.**



Probe: 10:1  
 Ch1: Connection- A50 TP DACOUT  
 Coupling- dc  
 Ground- Center Graticule  
 Trigger: Internal Ch1  
 Slope- Positive

Figure 7-30 Correct Waveform At A50U401(6).

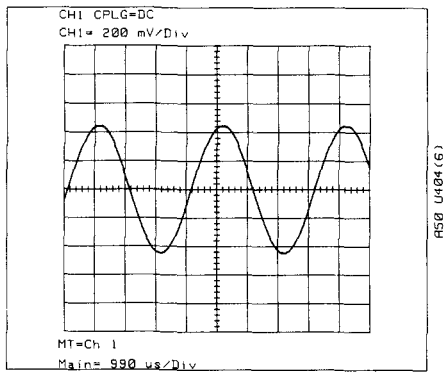


Probe: 10:1

Ch1: Connection- A50 U401(6)  
Coupling- dc  
Ground- Center Graticule

Trigger: Internal Ch1  
Slope- Positive

Figure 7-31 Correct Waveform At A50U404(6).

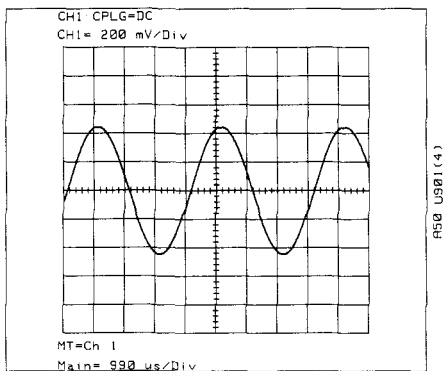


Probe: 10:1

Ch1: Connection- A50 U404(6)  
Coupling- dc  
Ground- Center Graticule

Trigger: Internal Ch1  
Slope- Positive

Figure 7-32 Correct Waveform At A50U901(4).



Probe: 10:1

Ch1: Connection- U901(4)  
Coupling- dc  
Ground- Center Graticule

Trigger: Internal Ch1  
Slope- Positive

**HP-IB I/O CIRCUITRY**

Test Routine 154 is used to troubleshoot the HP-IB circuitry. This test routine allows the processor to monitor the I/O pins of the HP-IB connector and display their status on the -hp-3561A CRT. While the test is running, the HP-IB connector pins must be shorted to ground one at a time. When this is done, the CRT display will so indicate. The HP-IB connector is located on the rear panel of the instrument.

Use the following procedure to initiate and operate Test Routine 154:

1. Program the -hp-3561A to run the test by pressing the following front panel keys:

```

PRESET
MODE ..... TEST SELECT.....154 ENTER
                START CONT TST

```

The CRT should indicate that Test 154 is in progress and to press the STOP TEST key to abort the test. The STOP TEST key must be pressed to exit this test! Failure to do this will result in -hp-3561A operating errors. The CRT should also display the HP-IB I/O connector signal names, pin numbers and pin state in six columns as shown next:

DIO1	1	0	0	13	DIO5
DIO2	2	0	0	14	DIO6
DIO3	3	0	0	15	DIO7
DIO4	4	0	0	16	DIO8
EOI	5	0	0	17	REN
DAV	6	0	0	18	GND
NRFD	7	0	0	19	GND
NDAC	8	0	0	20	GND
IFC	9	0	0	21	GND
SRQ	10	0	0	22	GND
ATN	11	0	0	23	GND
SHLD	12	0	0	24	IGND

Columns one and six identify the signal names, columns two and five identify the connector pin numbers and columns three and four identify the state of the pins (O indicates high, # indicates low).

2. Short the I/O pins to chassis ground one at a time. The shorted pin will cause the CRT to display a # instead of an O next to the corresponding pin number.

For example: Short connector pin number 1 to chassis ground. This will cause the CRT to display

DIO1	1	#	0	13	DIO5
------	---	---	---	----	------



No other pins should be affected. If any other pins are affected, ground U900(19). If the CRT indicates correctly, there is a short in the I/O connector, cable or U900. If other pins are still affected, the problem may be in U805.

3. Perform step 2 for the remaining signal pins with the exception of pin 11 ATN. Proceed to step 4 for this pin.

Note that the grounding of the IGND, GND and SHLD pins will not affect the CRT display. If there is a problem with all of the pins, U805 and/or U804 may be defective.

4. When pin 11, ATN, is grounded, the CRT will display the following:

DIO1	1	?	?	13	DIO5
DIO2	2	?	?	14	DIO6
DIO3	3	?	?	15	DIO7
DIO4	4	?	?	16	DIO8
EOI	5	?	?	17	REN
DAV	6	?	O	18	GND
NRFD	7	?	O	19	GND
NDAC	8	?	O	20	GND
IFC	9	?	O	21	GND
SRQ	10	?	O	22	GND
ATN	11	#	O	23	GND
SHLD	12	O	O	24	IGND

If not, ground U805(28). If the CRT display is correct, replace U903. If the CRT is still incorrect, the problem may be U805 and/or U804.

**Table 7-45 A50 Assembly Signal Connections**

**INPUTS**

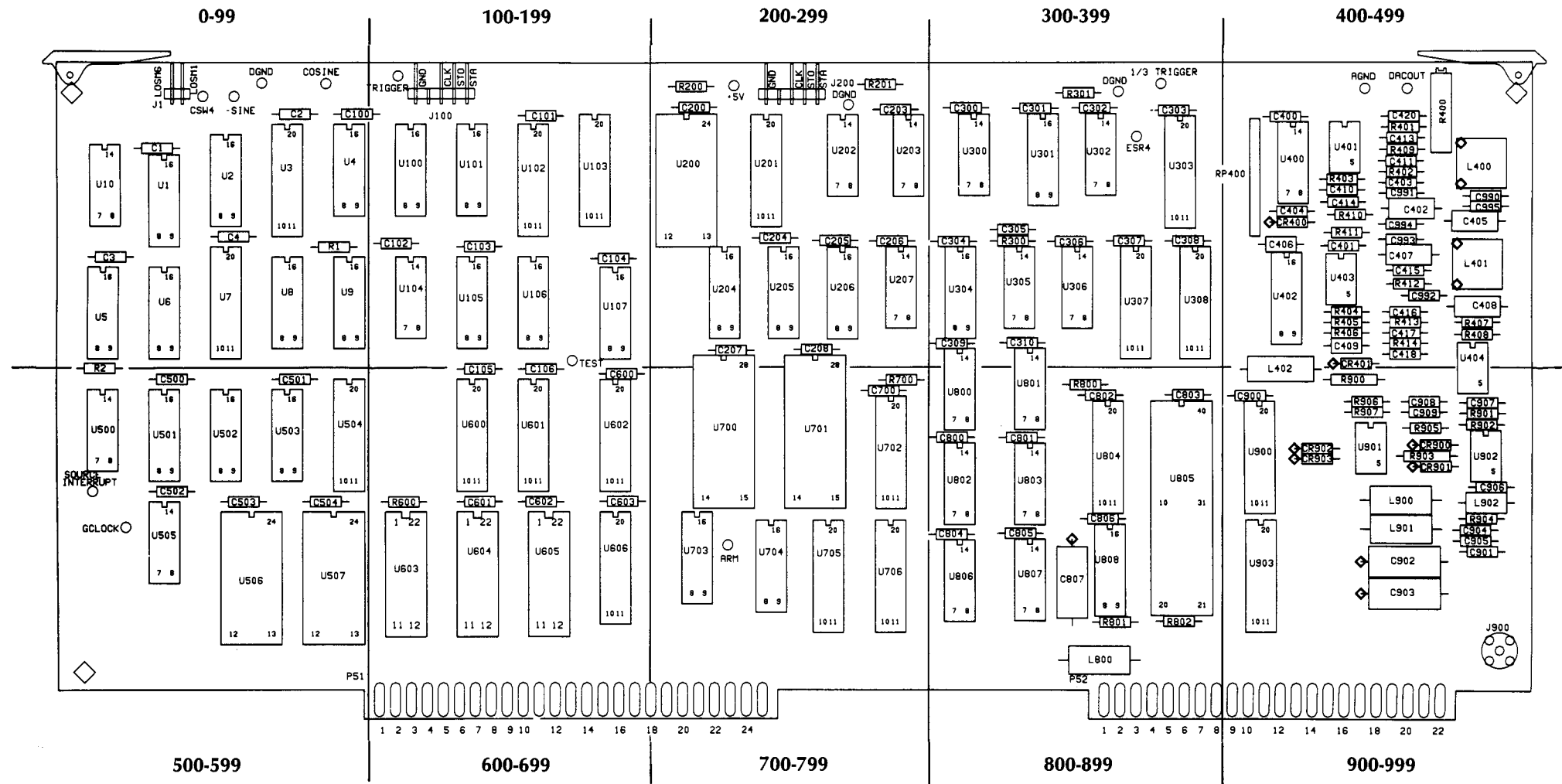
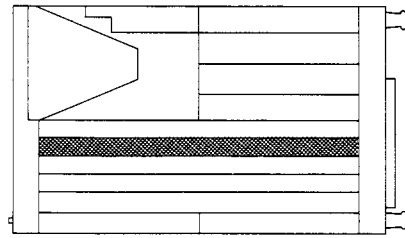
Signal Name	Functional Block	Connector Number	Origin Assembly
ESR*4	N	P51(B3)	A20
EXT TRIG	Y	P51(A8)	A82
HPIBS	GG	P51(A11)	A40
LOS	S	P51(A10)	A40
PBR/W	GG	P51(A13)	A40
PBUDS	GG	P51(B13)	A40
RESET	GG	P51(A3)	A40
SYNC2	K	P51(A5)	A20
ZPHTRIG	B	P51(A9)	A20
4 MHz	GG	P51(A2)	A40
10.24 MHz	K	P51(B2)	A20

**OUTPUTS**

Signal Name	Functional Block	Connector Number	Destination Assemblies
COSINE	L	P51(B8)	A20
HPCI	GG	P51(A7)	A40
HPDI	DD	P51(A6)	A40
NOISE	II	P52(B21)	A82
PRN_SYNC	EE	P52(A21)	A82
SINT	EE	P51(A12)	A40
-SINE	L	P51(A8)	A20

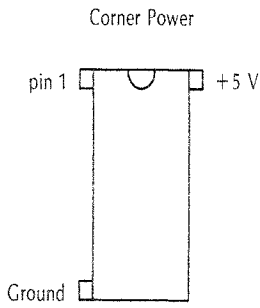
**I/O SIGNALS**

Signal Name	Functional Block	Connector Number	Destination Assembly
HPIB Data Bus DIO1 - DIO8	GG	P52(A11 - A14) P52(B11 - B14)	A82
HPIB I/O Control signals			
ATN	GG	P52(A18)	A82
DAV	GG	P52(B16)	A82
EOI	GG	P52(B15)	A82
IFC	GG	P52(A16)	A82
NDAC	GG	P52(B18)	A82
NRFD	GG	P52(B17)	A82
REN	GG	P52(A15)	A82
SRQ	GG	P52(A17)	A82
Processor Address Bus PAB0 - PAB2	GG	P52(A16,B15,B16)	A40, A60, A66/65
Processor Data Bus PDB0 - PDBF	A	P51(A17 - A24) P51(B17 - B24)	A30, A40, A60, A66/65

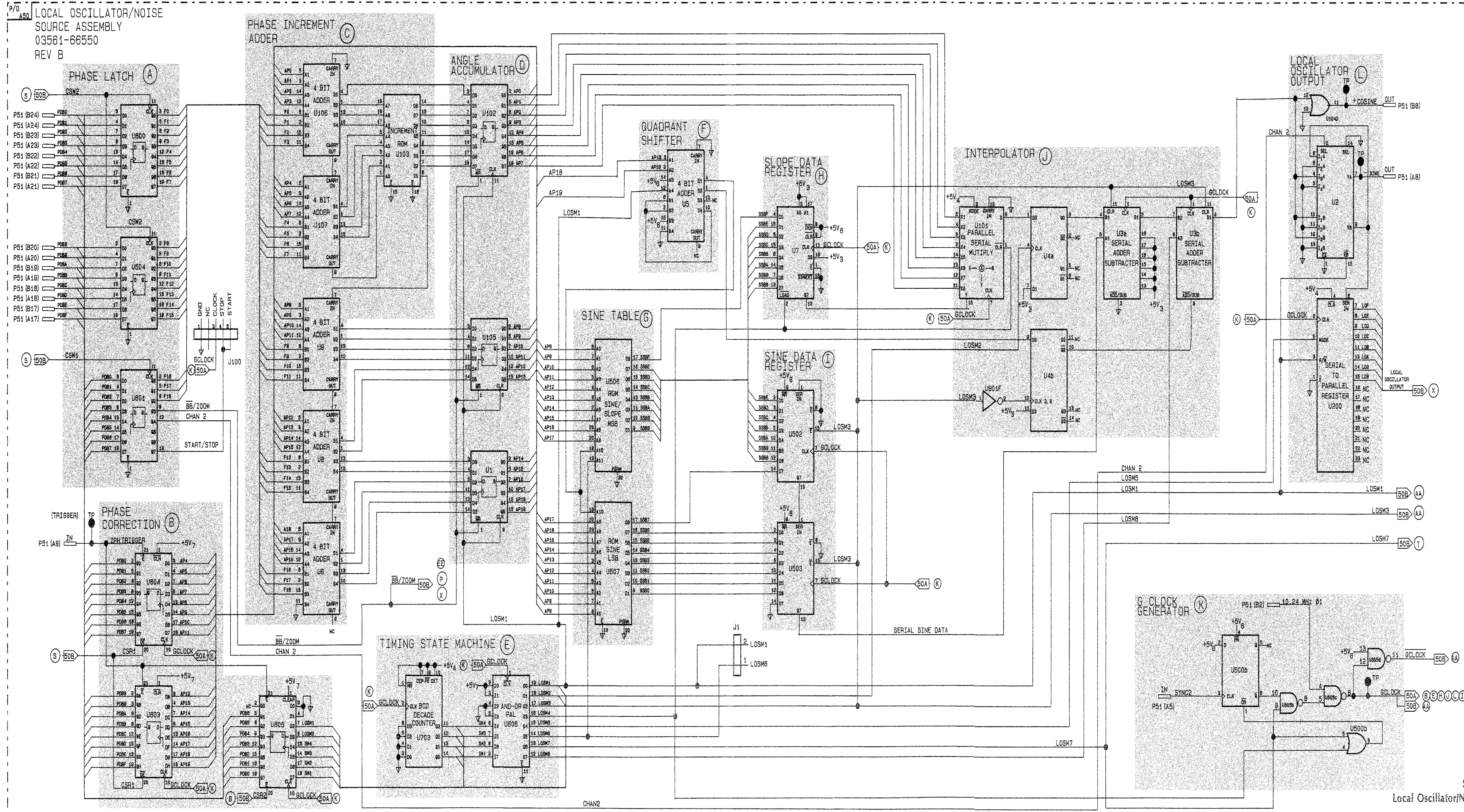


A50 Assembly

All integrated circuits are corner powered except those shown in the table below. Corner powered ICs have ground connected to the lower left pin, and +5 V connected to the upper right pin regardless of the total pin count. (eg, for a 16 pin DIP, ground is connected to pin 8 and +5 V is connected to pin 16)

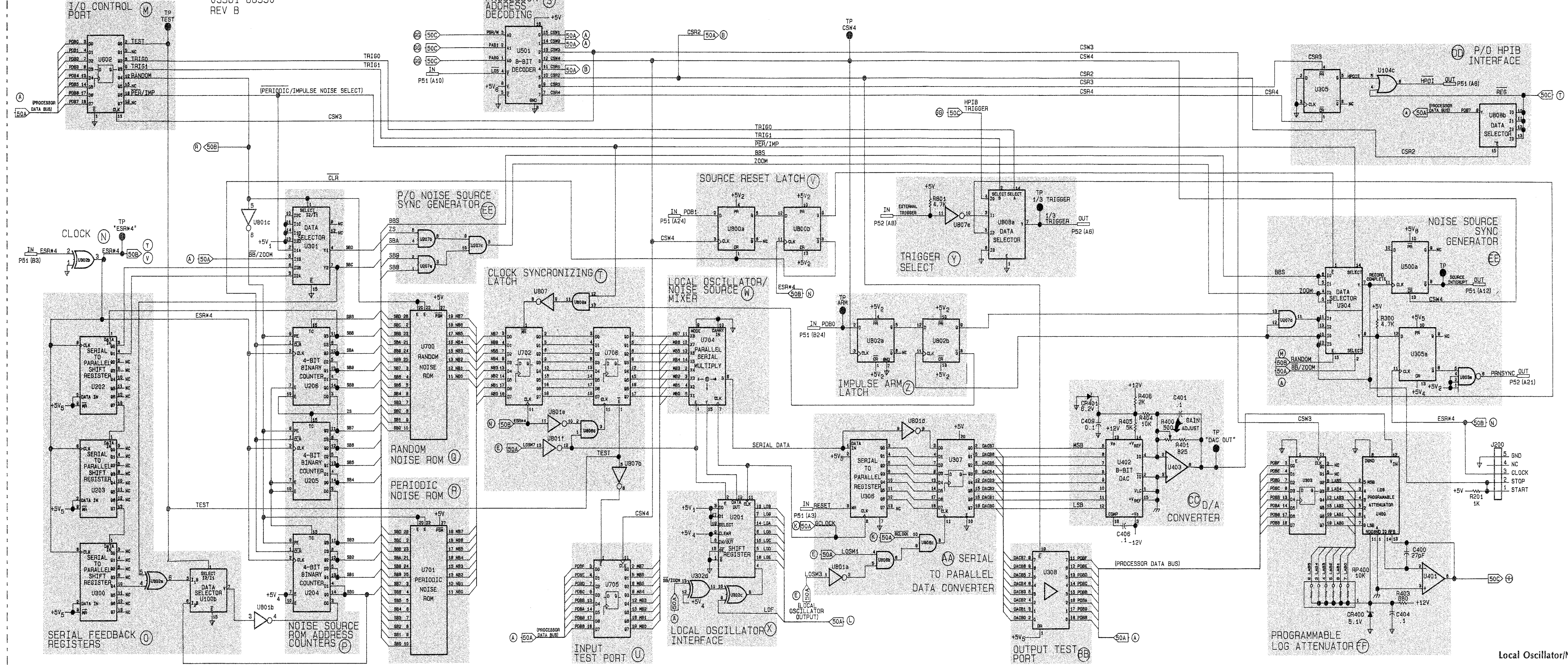


	+12V	+12V <sub>1</sub>	+12V <sub>2</sub>	+12V <sub>3</sub>	+12V <sub>4</sub>	-12V	-12V <sub>1</sub>	-12V <sub>2</sub>	-12V <sub>3</sub>	-12V <sub>4</sub>	+5V	GND
U401												
U402	13											
U403			7									
U404				7								
U506									4			24,21
U507												24,21
U805												40
U901	1											
U902		7										



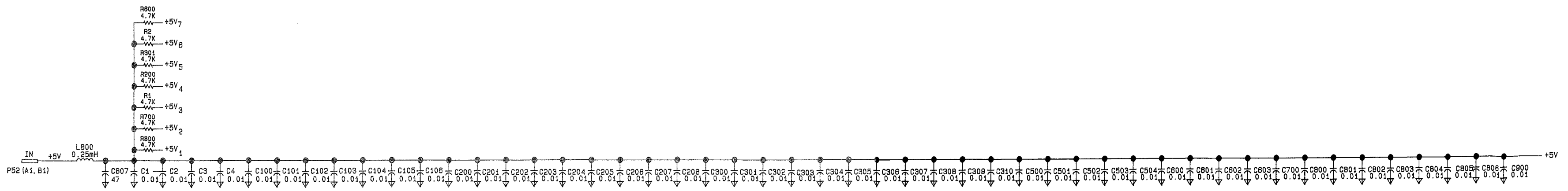
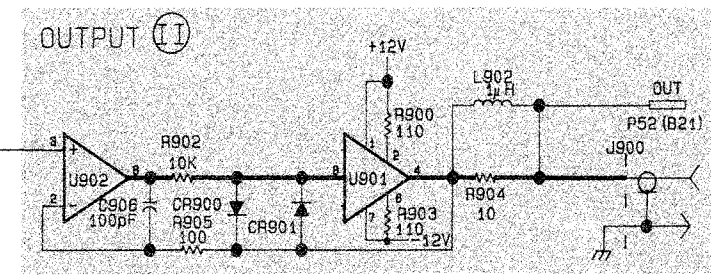
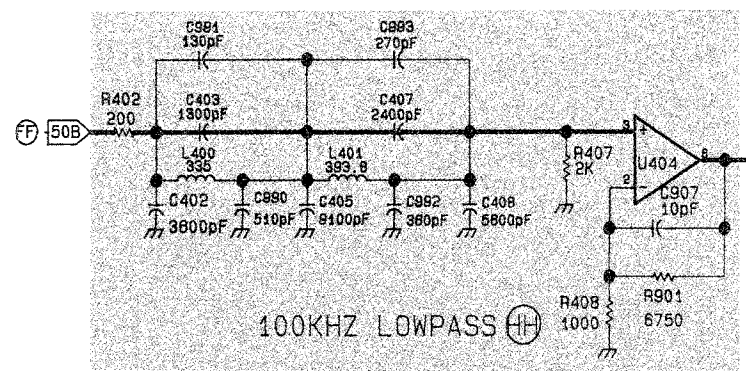
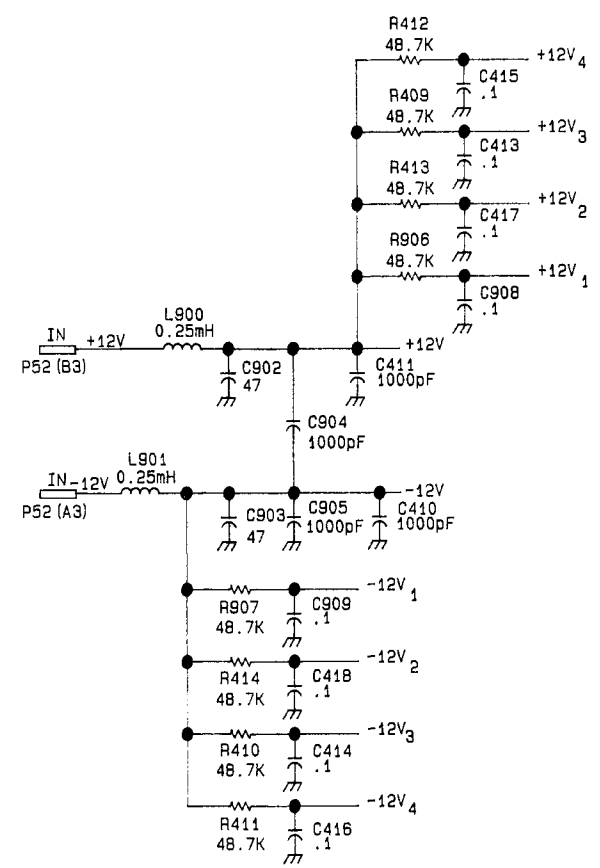
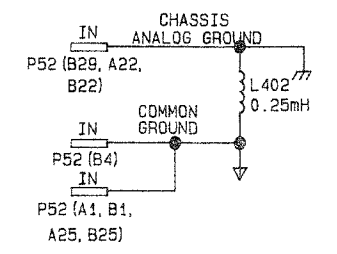
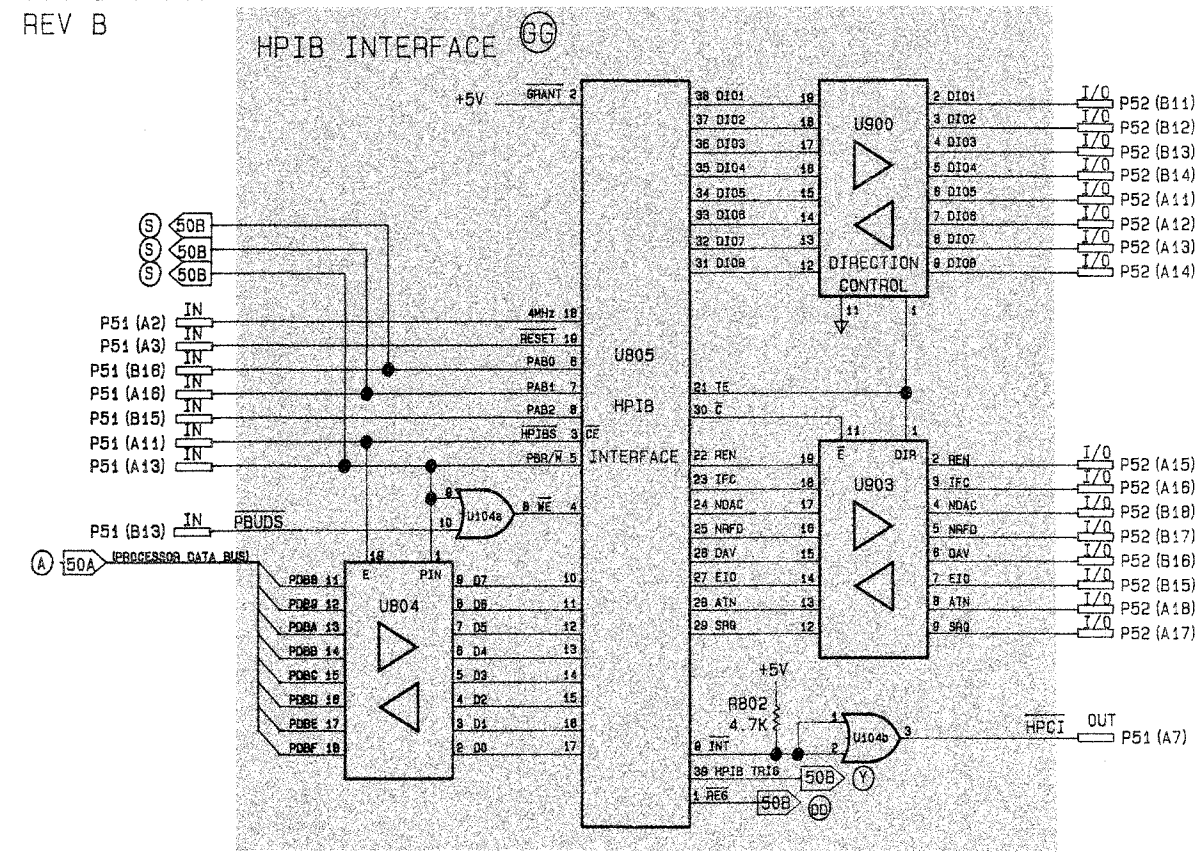
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Schematic A50B  
Local Oscillator/Noise Source Assembly  
7-1497-150

P/O A50 LOCAL OSCILLATOR/NOISE SOURCE ASSEMBLY  
 03561-66550  
 REV B



## **7-22 A60 DIGITAL DISPLAY DRIVER ASSEMBLY**

### **7-23 Digital Display Driver Circuit Description**

#### **GENERAL**

The -hp-3561A uses a raster scan CRT with a 512 horizontal (X), by 256 vertical (Y) grid screen. (128K total positions). Each grid position is called a pixel, and can be turned on or off by the display driver circuits. The digital display driver contains two 128k bit arrays of RAM; one array for the full bright display and one for the half bright display. Both the full bright display RAM and the half bright display RAM contain one memory location for each pixel on the CRT screen. A "1" stored in the memory location turns the pixel on and a "0" turns the pixel off. Graphics data is written into the display RAM as a series of lines. For each line the processor loads an X and Y axis start address, an X and Y axis increment value and a line length into the A60 Assembly. The A60 Assembly then uses these three values to generate all points of the line, and the addresses needed to store the line in RAM. Alpha-numeric data is directly stored into the RAM through the character writer circuit. Once data has been written into the display it remains there until the processor erases the display or writes new data over it. Display RAM bus cycles alternate between reading data out of RAM to update the CRT screen and writing new data from the processor into RAM. In this way the CRT screen is continuously updated.

#### **[A] INCREMENT REGISTER, [C] POSITION ADDRESS ADDER, [D] POSITION ADDRESS REGISTER**

When the processor writes a line to the display RAM these circuits generate the position address for each pixel of the line. The position address for successive points in the line is obtained by adding the X-increment and Y-increment values to the current X and Y position address.

#### **[B] RAM BYTE ADDRESS REGISTER, [F] RAM BIT ADDRESS REGISTER**

These circuits convert the position address register output into a RAM byte address and a RAM bit address. The bit address bus selects one of the eight RAMs in the selected RAM plane and the byte address bus addresses the specific location within the RAM. The byte address consists of two parts: a row address and a column address. The column address is taken from the upper seven bits of the position address register; the row address is taken from the next seven bits. The bottom three bits of the position address register are decoded to form the bit address bus.



**[G] MODE CONTROL LATCH, [I] RAM DATA WRITER, [J] CHARACTER WRITER**

These circuits generate the data which is stored into the memory location selected by the position address register. Data can be stored into RAM from five different sources. The data source is selected by the processor through the mode control signals M0, M1, and M2. The character writer is selected only when the processor is writing alphanumeric data directly into the display RAM.

Mode Control Signals			Data Source Selected U804	
M0	M1	M2	Pin#	Description
0	0	0	4	Write a "0" into RAM; erases the CRT screen at the selected address.
0	0	1	3	Copy the current RAM data at the selected address.
0	1	0	2	Invert the current RAM data at the selected address.
0	1	1	1	Write a "1" into RAM; turns the CRT screen on at the selected address.
1	X	X	12 13 14 15	Write data from the character register into the selected address.

**[K] FREE RUN/LINE SYNC TIMING, [L] COLUMN ADDRESS COUNTER, [M] ROW ADDRESS COUNTER**

These circuits access the display RAM on every other bus cycle to continuously refresh and update the pattern on the CRT screen. The rate at which the CRT screen is updated is determined by the free run/line sync circuit. When A60J200 is in the sync position the refresh rate is determined by the LSYNC signal, which is locked to the power line frequency. When A60J200 is in the free run position, the refresh rate is fixed at 62.8 Hz. The row address counter and the column address counter cycle through all memory locations for each pattern refresh.

**[N] RAM PLANE 1, [O] RAM PLANE 2**

Each RAM is a 16k by 1 bit dynamic RAM. The RAM is addressed in a two step process. In the first step, a seven bit row address is latched into the RAM, and in the second step, a seven bit column address is latched into the RAM. The RAM then internally combines these addresses to obtain the location address.



**[S] RAM DATA READER**

To refresh the CRT screen, the RAM data reader transfers data from the display RAM to the CRT cathode drive circuit. The data is read from the RAM address generated by the row and column address counters. At each address, the BYTE WRITE signal is used to read one bit of data from each of the eight RAMs in plane 1 to generate the VIDF signal, and one bit of data from each of the RAMs in plane 2 to generate the VIDH signal.

**[R] FSYNC/SSYNC TIMING**

This circuit uses the address counter outputs to generate the CRT vertical and horizontal sweep signals. The slow sync signal (SSYNC) triggers a horizontal sweep and the fast sync signal (FSYNC) triggers a vertical sweep. A new vertical sweep is generated each time the row address counter reaches a count of 38. A new horizontal sweep is generated each time the column address counter reaches its highest count.

**[P] COPY/COMPLIMENT DATA FEEDBACK, [Q] PROCESSOR DATA REGISTER**

Through these registers, the data in RAM can be read out and transferred back to the RAM data writer. The RAM data writer can then either copy the data directly back into RAM or compliment the data before writing it back into RAM. Through the processor data register, the processor may read the data stored in the display RAM. This is used only for the the display RAM test at power on.

**[T] LINE LENGTH COUNTER**

This counter determines the length of the line to be written to the CRT screen. The processor loads the counter with a value equal to the full count minus the line length. When the counter reaches full count a carry is generated ( $\overline{CDONE}$ ). The  $\overline{CDONE}$  signal clears the position address and stops the line write timing generator.

**[W] TIMING GENERATOR, [U] LINE WRITE TIMING GENERATOR  
[X] RAM ROW ADDRESS STROBE TIMING**

These circuits generate all of the timing signals used to generate a line and store it in the display RAM. The line write timing generator starts a sequence when the processor loads the Y increment register and stops when the line length counter issues a  $\overline{CDONE}$  signal.

**Table 7-46 A60 Assembly Signal Descriptions**

<b>Signal</b>	<b>Description</b>
BIT/BYTE	Low when only one bit of data is being written to or read from the RAM. High to write identical data to all eight RAMs in a plane.
BITCLK	BIT CLoCK: Clocks the RAM data into the analog display driver through the RAM data reader.
$\overline{\text{CDONE}}$	Counter DONE: Issued by the line length counter to indicate that the line is complete.
$\overline{\text{CAS}}$	Column Address Strobe: Clocks the column address into the RAM.
$\overline{\text{CLK}}$	Character CLoCK: High to enable a read from RAM and low to enable a write to RAM.
$\overline{\text{CRTON}}$	Low to turn the CRT on.
$\overline{\text{CTSEL}}$	CounTer SEL: Loads the line length data into the line length counter.
$\overline{\text{DDBCLK}}$	Display Data FeedBack CLoCK: Latches the RAM output data into the feedback register.
$\overline{\text{DNCLK}}$	Down CLoCK: Increments the line length counter and the position address counter by one.
$\overline{\text{DSPH}}$	DiSPlay Holdoff: Indicates to the processor that the current data transfer is complete. This signal also starts the line length timing generator.
$\overline{\text{DSPS}}$	DiSPlay Select: Used by the processor to address the A60 Assembly.
FSYNC	Fast Sweep SYNCRonizer: Synchronizes the CRT vertical sweep with the horizontal sweep and the CRT video data.
LSYNC	Line SYNCRonizer: Synchronizes the CRT refresh rate to the power line frequency.
PW1, PW2	Plane 1 Write, Plane 2 Write: Programmed by the processor to indicate which RAM plane the data should be written to. Only one of these lines is active at a time.
R/C	Row/Column Address: Low to select the RAM row address on the byte address bus.
R/C	Row/Column Address: Low to select the RAM column address on the byte address bus.
RAS1 RAS2	Ram Address Strobe PLANE1: Clocks the row address into RAM (PLANE1 or PLANE2).
SSYNC	Slow SYNCRonizer: Synchronizes the CRT horizontal sweep to the vertical sweep and to the video data.
SSYNCE	Slow SYNCRonizer Enable: Enables a SSYNC signal when the column address counter reaches its highest count.

**Table 7-46 A60 Assembly Signal Descriptions (Cont'd)**

VIDF	VIDeo Full Bright Data: Full bright (PLANE1) RAM data to drive the CRT cathode.
VIDH	VIDeo Half Bright Data: Half bright (PLANE2) RAM data to drive the CRT cathode.
XINC	X-axis INCrement: Loads data into the X-axis increment register.
XSEL	X-axis SElect: Enables data to be clocked into the X-axis increment register.
YINC	Y-axis INCrement: Loads data into the Y-axis increment register, and triggers the line write timing generator to start writing a line to RAM.
YSEL	Y-axis SElect: Enables data to be clocked into the X-axis increment register.

**7-24 Troubleshooting the Digital Display Driver**

**GENERAL**

All of the circuits on the A60 Assembly, except the processor interface circuits and the RAM, can be tested with the A60J100 jumper test. The A60J100 jumper test can be run with only the power supply and the A60 Assemblies installed in the the -hp-3561A. The A40W1 jumper test is used to troubleshoot the processor interface circuits, and the power-on test is used to troubleshoot the RAM. These two tests require an operational A40 Assembly to be installed in the -hp-3561A. Failures occurring on the alpha-numerics only are most likely the character writer.

Troubleshoot the circuits on the A60 Assembly in the order given in Table 7-47. In this table, level one circuits must be operational before level two circuits can be tested, etcetera.

**Table 7-47 A60 Circuit Troubleshooting Order**

Level	Functional Blocks
1	Test Control Circuit: H Timing Circuits: U, V, W, X
2	RAM Address Generation Circuits: C, D, E, F CRT Refresh Timing Circuits: K, L, M, R
3	RAM: N, O
4	RAM Data Reader: S
5	Processor Interface Circuits: A, B, G, J, T, Y

**[H] Test Control**

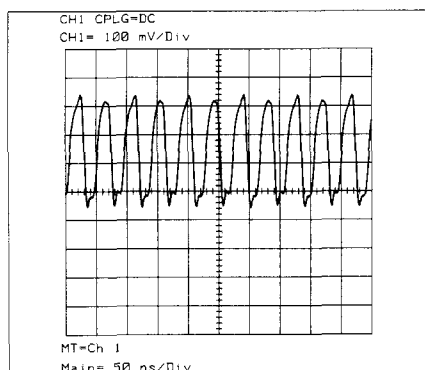
1. Turn the -hp-3561A LINE power switch OFF.
2. Move the A60J100 test jumper to the PLANE1 test position and place the A60 Assembly on an extender board.
3. Turn the -hp-3561A LINE power switch ON.
4. Check the following signals.

U1(8)	TTL high
U205(10)	0 V
U304(3,6,8)	TTL high
U305(5)	TTL high
U401(6)	0 V
U304(3)	TTL high
U805(3)	TTL high
U900(5,9)	TTL high

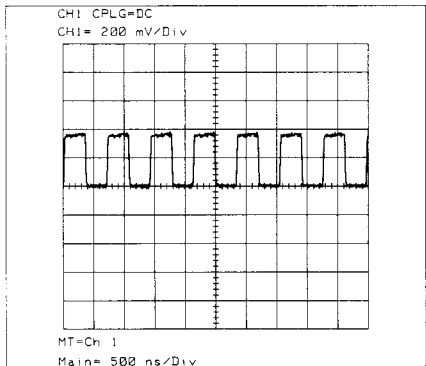
**[U] LINE WRITE TIMING GENERATOR, [V] DISPLAY CLOCK, [W] TIMING GENERATOR, [X] RAM ROW ADDRESS STROBE TIMING**

To troubleshoot these circuits move the A60J100 test jumper to the PLANE1 test position and check the waveforms given in Figure 7-33.

**Figure 7-33 Clock and Timing Waveforms**



Probe: 10:1  
 Ch1: Connection- A60 TP308 "22.589 MHz"  
 Coupling- dc  
 Ground- Center Graticule  
 Trigger: Internal- Ch1  
 Slope- Positive  
 Bandwidth Limit: OFF

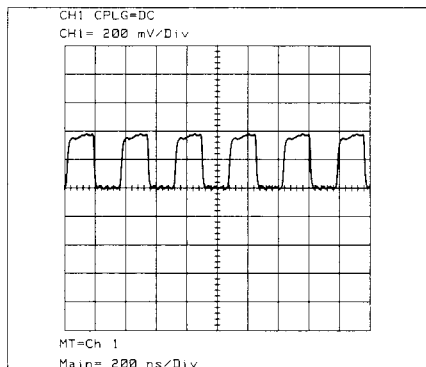


Probe: 10:1

Ch1: Connection- A60 U400(11) "CLK"  
 Coupling- dc  
 Ground- Center Graticule

Trigger: Internal- Ch1  
 Slope- Positive

Bandwidth Limit: ON

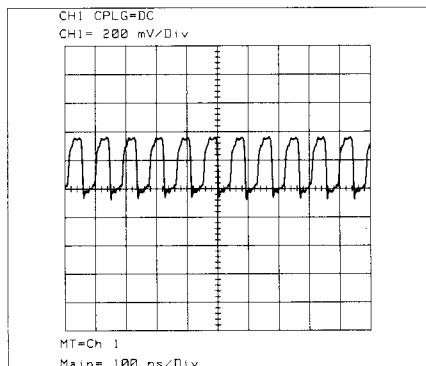


Probe: 10:1

Ch1: Connection- A60 U400(12)  
 Coupling- dc  
 Ground- Center Graticule

Trigger: Internal- Ch1  
 Slope- Positive

Bandwidth Limit: ON

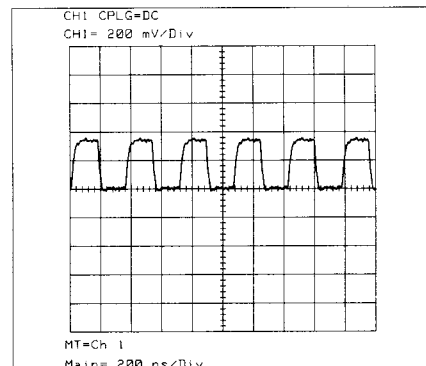


Probe: 10:1

Ch1: Connection- A60 U400(14) "BITCLK"  
 Coupling- dc  
 Ground- Center Graticule

Trigger: Internal- Ch1  
 Slope- Positive

Bandwidth Limit: OFF



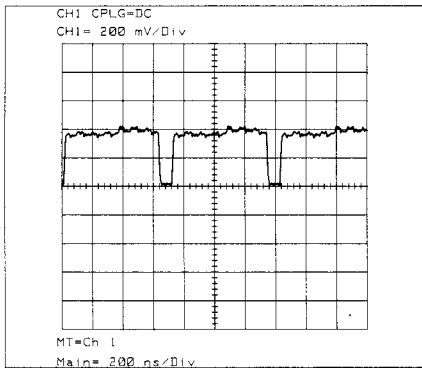
Probe: 10:1

Ch1: Connection- A60 U803(4)  
 A60 U803(5) "R/C"  
 A60 U803(10)  
 A60 U803(12) "R/C"  
 A60 U803(13) "CAS"

Coupling- dc  
 Ground- Center Graticule

Trigger: Internal- Ch1  
 Slope- Positive

Bandwidth Limit: ON

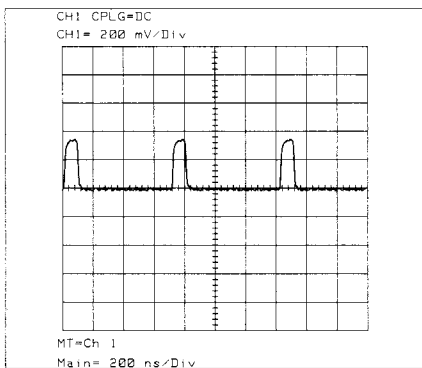


Probe: 10:1

Ch1: Connection- A60 U305(8) "S/L"  
Coupling- dc  
Ground- Center Graticule

Trigger: Internal- Ch1  
Slope- Positive

Bandwidth Limit: ON

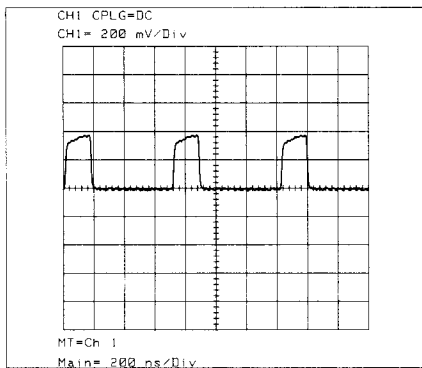


Probe: 10:1

Ch1: Connection- A60 U901(6) "DNCLK"  
Coupling- dc  
Ground- Center Graticule

Trigger: Internal- Ch1  
Slope- Positive

Bandwidth Limit: ON

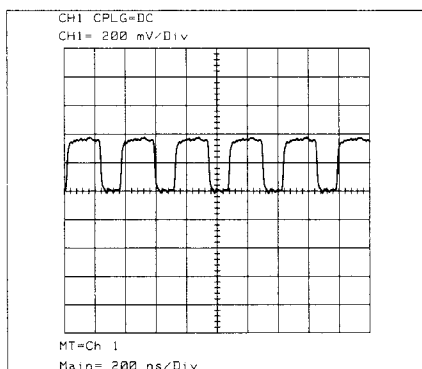


Probe: 10:1

Ch1: Connection- A60 U901(12) "PIXEN"  
Coupling- dc  
Ground- Center Graticule

Trigger: Internal- Ch1  
Slope- Positive

Bandwidth Limit: ON

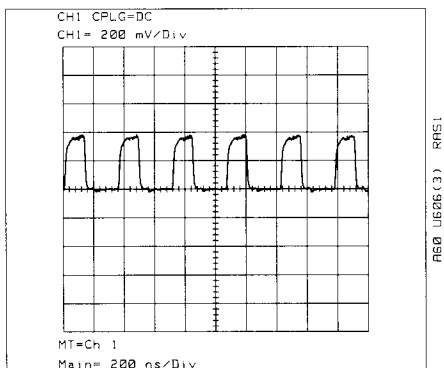


Probe: 10:1

Ch1: Connection- A60U805(8) "RAS"  
Coupling- dc  
Ground- Center Graticule

Trigger: Internal- Ch1  
Slope- Positive

Bandwidth Limit: ON

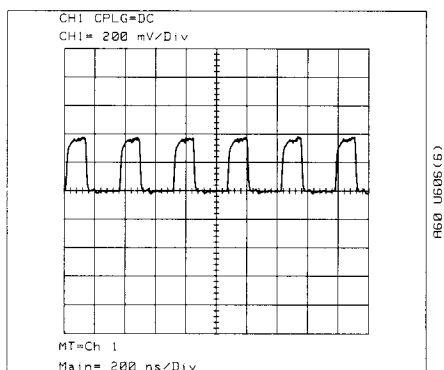


Probe: 10:1

Ch1: Connection- A60U606(3) "RAS1"  
Coupling- dc  
Ground- Center Graticule

Trigger: Internal- Ch1  
Slope- Positive

Bandwidth Limit: ON



Probe: 10:1

Ch1: Connection- A60U606(6) "RAS2"  
Coupling- dc  
Ground- Center Graticule

Trigger: Internal- Ch1  
Slope- Positive

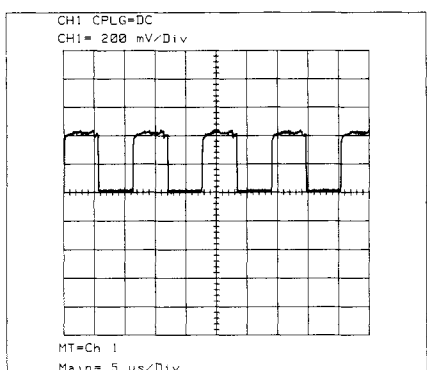
Bandwidth Limit: ON

**[C] POSITION ADDRESS ADDER, [D] POSITION ADDRESS REGISTER, [E] RAM BYTE ADDRESS REGISTER, [F] RAM BIT ADDRESS REGISTER**

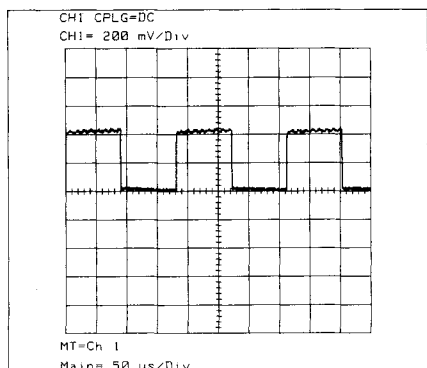
Move the A60J100 test jumper to the PLANE1 test position and check the waveforms given in Figure 7-34. These waveforms should be checked starting with the least significant bit (PXB0) and proceeding to the most significant bit (PXB16).

If these waveforms are correct, check the signatures given in Table 7-48.

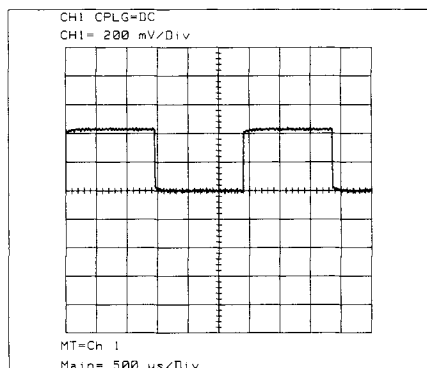
**Figure 7-34 Position Address Waveforms**



Probe: 10:1  
 Ch1: Connection- A60 TP102 "PXB3"  
 A60 U700(10)  
 Coupling- dc  
 Ground- Center Graticule  
 Trigger: Internal- Ch1  
 Slope- Positive  
 Bandwidth Limit: OFF

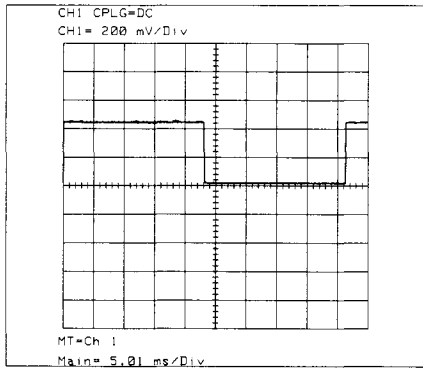


Probe: 10:1  
 Ch1: Connection- A60 TP200 "PXB7"  
 A60 U208(10)  
 Coupling- dc  
 Ground- Center Graticule  
 Trigger: Internal- Ch1  
 Slope- Positive  
 Bandwidth Limit: ON



Probe: 10:1  
 Ch1: Connection- A60 TP300 "PXB11"  
 A60 U207(10)  
 Coupling- dc  
 Ground- Center Graticule  
 Trigger: Internal- Ch1  
 Slope- Positive  
 Bandwidth Limit: ON



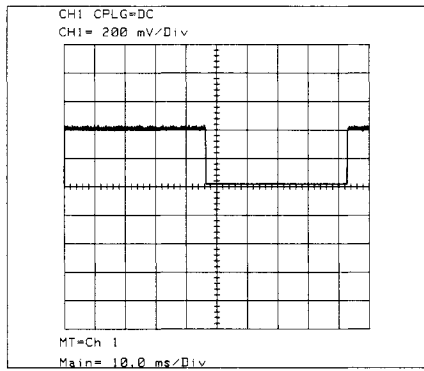


Probe: 10:1

Ch1: Connection- A60 U105(2) "PXB15"  
A60 U206(10)  
Coupling- dc  
Ground- Center Graticule

Trigger: Internal- Ch1  
Slope- Positive

Bandwidth Limit: OFF

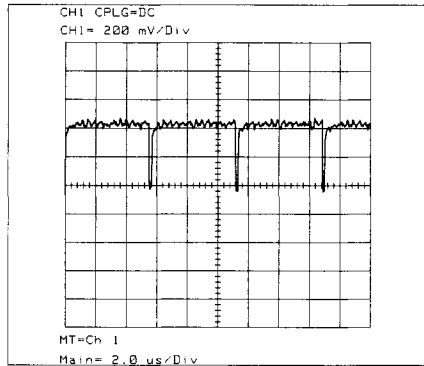


Probe: 10:1

Ch1: Connection- A60 TP100 "PXB16"  
A60 U300(8)  
Coupling- dc  
Ground- Center Graticule

Trigger: Internal- Ch1  
Slope- Positive

Bandwidth Limit: ON



Probe: 10:1




Ch1: Connection- A60 U702(7, 9, 10, 11, 12,  
13, 14 ,15)  
A60 U600(3, 6, 8, 11)  
A60 U601(3, 6, 8, 11)

Coupling- dc  
Ground- Center Graticule

Trigger: Internal- Ch1  
Slope- Positive

Bandwidth Limit: ON

**Table 7-48 RAM Byte Address and Bit Address Signatures**

Signal	Polarity	Connection
Clock		A60 U106(1) "CLK"
Start		A60 TP100 "PXB16"
Stop		A60 TP100 "PXB16"
+ 5 V Signature - 0003		
RAM Byte Address Register		
U104(3)	7791	
U104(5)	0356	
U104(7)	U759	
U104(9)	6F9A	
U104(13)	P763	
U104(15)	1UP5	
U104(17)	8484	

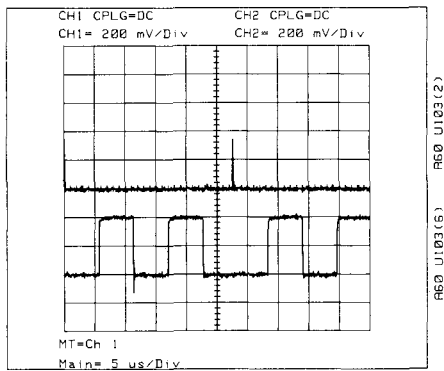
**[K] FREE RUN/LINE SYNC TIMING, [L] COLUMN ADDRESS COUNTER,  
[M] ROW ADDRESS COUNTER, [R] FSYNC/SSYNC TIMING**

Move the A60J100 test jumper to the PLANE1 test position and the A60J200 test jumper to the 60 Hz position. Check the waveforms given in Figure 7-35. These waveforms should be checked starting with the least significant bit of the row address counter (U103(3)) and proceeding to the most significant bit of the column address counter (U200(10)).

Move the A60J200 test jumper back to the SYNC position.

If all of the waveforms given in Figure 7-35 are correct, check the signatures given in Table 7-49.

Figure 7-35 Row and Column Address Counter Waveforms



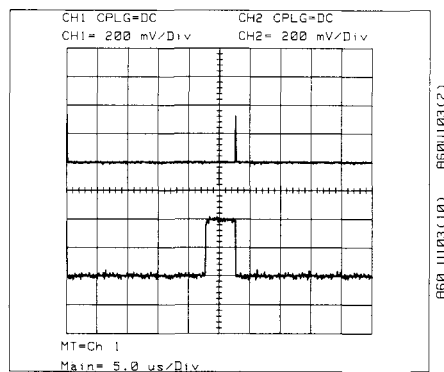
Probe: 10:1

Ch1: Connection- A60 U103(2)  
Coupling- dc  
Ground- Center Graticule

Ch2: Connection- A60 U103(6)  
Coupling- dc  
Ground- Second Graticule from Bottom

Trigger: Internal- Ch1  
Slope- Positive

Bandwidth Limit: OFF



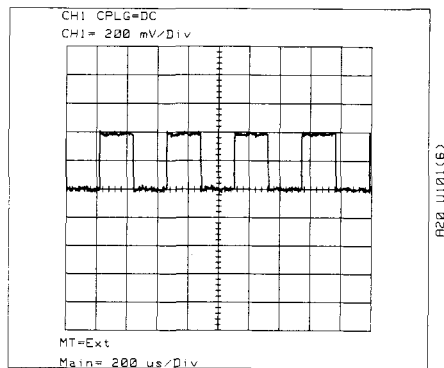
Probe: 10:1

Ch1: Connection- A60 U103(2)  
Coupling- dc  
Ground- Center Graticule

Ch2: Connection- A60 U103(10)  
Coupling- dc  
Ground- Second Graticule from Bottom

Trigger: Internal- Ch1  
Slope- Positive

Bandwidth Limit: OFF

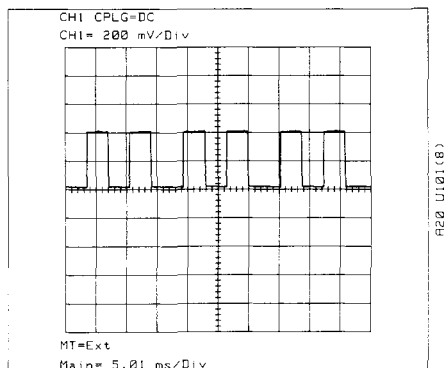


Probe: 10:1

Ch1: Connection- A60 U101(6)  
Coupling- dc  
Ground- Center Graticule

Trigger: External- A60 U101(2)  
Slope- Positive

Bandwidth Limit: OFF

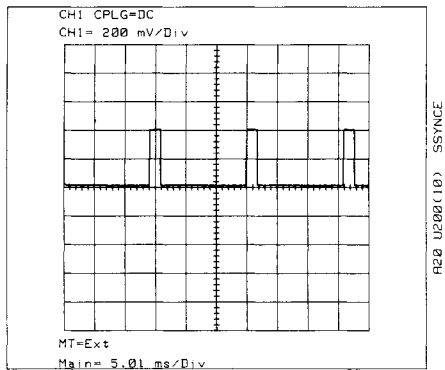


Probe: 10:1

Ch1: Connection- A60 U101(8)  
Coupling- dc  
Ground- Center Graticule

Trigger: External- A60 U101(2)  
Slope- Positive

Bandwidth Limit: OFF

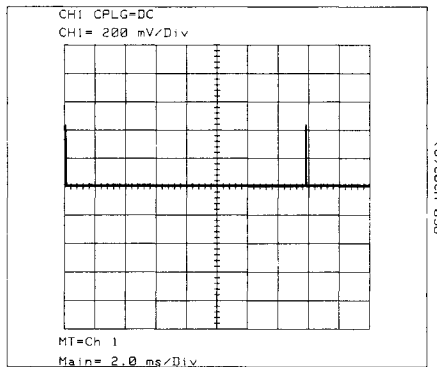


Probe: 10:1

Ch1: Connection- A60 U200(10) "SSYNCE"  
Coupling- dc  
Ground- Center Graticule

Trigger: External- A60 U101(2)  
Slope- Positive

Bandwidth Limit: OFF

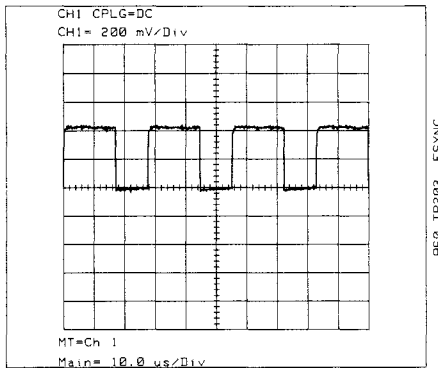


Probe: 10:1

Ch1: Connection- A60 U303(8)  
Coupling- dc  
Ground- Center Graticule

Trigger: Internal- Ch1  
Slope- Positive

Bandwidth Limit: ON

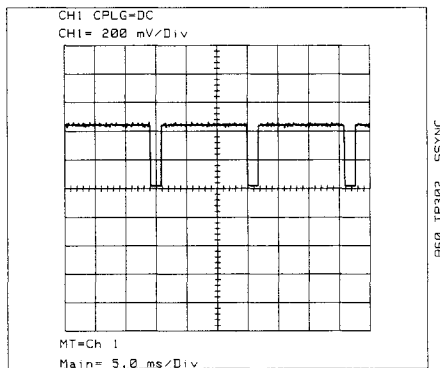


Probe: 10:1

Ch1: Connection- A60 TP203 "FSYNC"  
Coupling- dc  
Ground- Center Graticule

Trigger: Internal- Ch1  
Slope- Positive

Bandwidth Limit: OFF






Probe: 10:1

Ch1: Connection- A60 TP302 "SSYNC"  
Coupling- dc  
Ground- Center Graticule

Trigger: Internal- Ch1  
Slope- Positive

Bandwidth Limit: ON

**Table 7-49 RAM Address Signatures**

Signal	Polarity	Connection
Clock		A60 U100(19) "CLK"
Start		A60 U200(10) "SSYNCE"
Stop		A60 U200(10) "SSYNCE"
+ 5 V Signature - 5F52		
U100(3)	AF98	
U100(5)	C74H	
U100(7)	AF1C	
U100(9)	8641	
U100(13)	CH3C	
U100(15)	77H9	
U100(17)	4H8U	

**[N] RAM PLANE1 (FULL BRIGHT), [O] RAM PLANE2 (HALF BRIGHT)**

Troubleshoot the RAM circuits using the -hp-3561A power-on test. The A60J100 test jumper should be in the run position for this test. Table 7-50 lists the power-on test return codes and the corresponding failed RAM. If the power-on test indicates a failure in several RAMs, the most likely cause of the failure is the copy compliment data feedback registers or the processor data register.

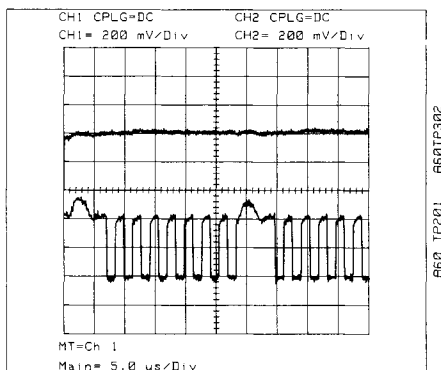
**Table 7-50 Power Or Test Return Codes for the Display RAM**

Return Code	Chip Code	Failed RAM
0 7 28	G	U507
0 7 28	H	U505
0 7 28	J	U503
0 7 28	K	U501
0 7 28	L	U9
0 7 28	M	U7
0 7 28	N	U5
0 7 28	P	U3
0 7 28	R	U506
0 7 28	T	U504
0 7 28	U	U502
0 7 28	V	U500
0 7 28	W	U8
0 7 28	X	U6
0 7 28	Y	U4
0 7 28	Z	U2

**[S] RAM DATA READER**

1. Move the A60J100 test jumper to the PLANE1 test position and the A60J200 test jumper to the 60 Hz position. Check the waveform at A60TP201 as shown in Figure 7-36.
2. Move the A60J100 test jumper to the PLANE2 test position and check the waveform at A60TP202 as shown in Figure 7-36.
3. Move the A60J200 test jumper back to the SYNC position.

**Figure 7-36 RAM Data Reader Waveforms**



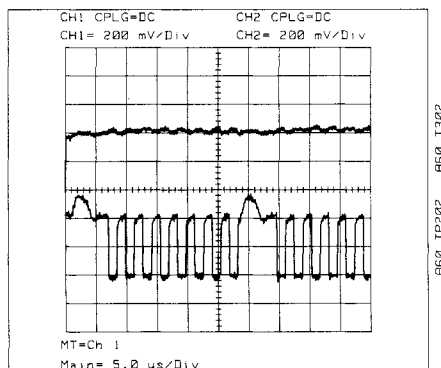
Probe: 10:1

Ch1: Connection- A60 TP302 "SSYNC"  
Coupling- dc  
Ground- Center Graticule

Ch2: Connection- A60 TP201 "VIDF"  
Coupling- dc  
Ground- Center Graticule

Trigger: Internal- Ch1  
Slope- Positive

Bandwidth Limit: ON



Probe: 10:1

Ch1: Connection- A60 TP302 "SSYNC"  
Coupling- dc  
Ground- Center Graticule

Ch2: Connection- A60 TP202 "VIDH"  
Coupling- dc  
Ground- Center Graticule

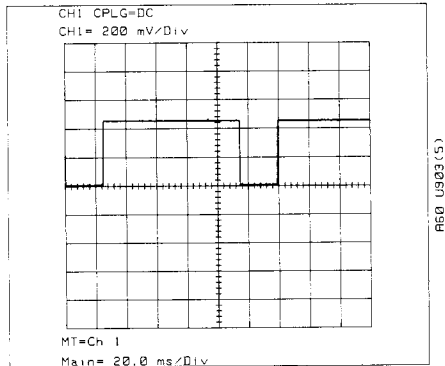
Trigger: Internal- Ch1  
Slope- Positive

Bandwidth Limit: ON

**[A] INCREMENT REGISTER, [B] ADDRESS DECODER, [G] MODE CONTROL LATCH  
[J] CHARACTER WRITER, [T] LINE LENGTH COUNTER, [Y] BEEPER TIMING**

1. Turn the -hp-3561A LINE power switch OFF.
2. Move test jumper A40W1 on the A40 Assembly to the test position.
3. Move test jumper A60J100 on the A60 Assembly to the run position.
4. Turn the -hp-3561A LINE power switch ON. When the front panel LEDs begin to blink (approximately seconds after power-on), check the signatures given in Table 7-51 and the waveforms given in Figure 7-37.

**Figure 7-37 Beeper Timing Waveforms**

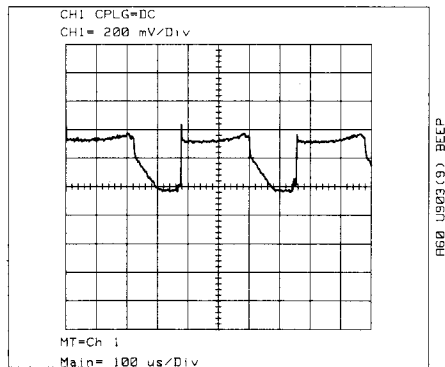


Probe: 10:1

Ch1: Connection- A60 U903(5)  
Coupling- dc  
Ground- Center Graticule

Trigger: Internal- Ch1  
Slope- Negative

Bandwidth Limit: ON



Probe: 10:1




Ch1: Connection- A60 U903(9) "BEEP"  
Coupling- dc  
Ground- Center Graticule

Trigger: Internal- Ch1  
Slope- Positive

Bandwidth Limit: ON

Note: This waveform will appear to jitter.

**Table 7-51 A60 Processor Interface Signatures**

Signature Analyzer Setup Signal	Polarity	Connection	
Clock		A60 U806(4) " $\overline{\text{DSPS}}$ "	
Start		A40CR1 (Cathode of Green LED)	
Stop		A40CR1 (Cathode of Green LED)	
+ 5 V Signature - AU96			
Address Decoder		Increment Register	
U303(3)	AP3H	U209(2)	9747
U303(6)	C232	U209(5)	59F5
U806(7)	4304	U209(6)	A8A2
U806(9)	9FU5	U209(9)	3052
U806(10)	A205	U209(12)	UPUP
U806(11)	PA07	U209(15)	H938
U806(12)	C23H	U209(16)	456H
U806(13)	FP6H	U209(19)	9H2P
U806(14)	U7A3		
U806(15)	C396	U302(5)	A36U
Mode Control Latch		U304(3)	A171
U800(2)	P852	U701(2)	4HUP
U800(5)	H766	U701(5)	F5U2
U800(6)	5967	U701(6)	6504
U800(9)	A1AA	U701(9)	A171
U800(12)	9P18	U701(12)	CF35
U800(15)	06P3	U701(15)	0A70
U800(16)	6520	U701(16)	P800
U800(19)		U701(19)	2142
U304(6)	H766		
U304(8)	5967		

**Table 7-52 A60 Assembly Signal Connections**

**INPUTS**

Signal Name	Functional Block	Connector Number	Origin Assembly
$\overline{\text{DSPS}}$	B	P61(A8)	A40
$\overline{\text{LSYNC}}$	K	P62(B9)	A71
$\overline{\text{PBR/W}}$	Q	P61(A13)	A40
$\overline{\text{RESET}}$	H	P61(A3)	A40



**OUTPUTS**

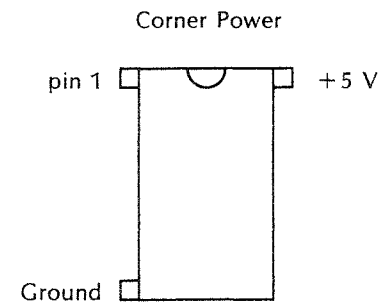
<b>Signal Name</b>	<b>Functional Block</b>	<b>Connector Number</b>	<b>Destination Assembly</b>
BEEP	Y	P62(B8)	A72
DSPH	U	P61(A7)	A40
FSYNC	R	P61(B4)	A90
SSYNC	R	P61(B5)	A90
VIDF	S	P61(B3)	A90
VIDH	S	P61(B2)	A90

**I/O SIGNALS**

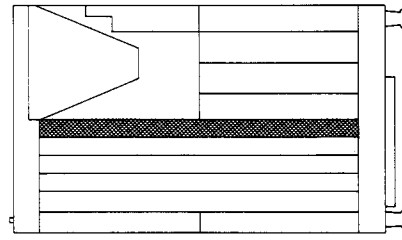
<b>Signal Name</b>	<b>Functional Block</b>	<b>Connector Number</b>	<b>Destination Assemblies</b>
Processor Address Bus PAB0 - PAB2	B	P61(A16,B15,B16)	A40, A50, A66/65 A81
Processor Data Bus PDB0 - PDBF	A,Q	P61(A17 - A24) P61(B17 - B24)	A30, A40, A50 A66/65, A80

### A60 Assembly

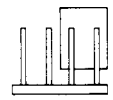
All integrated circuits are corner powered except those shown in the table below. Corner powered ICs have ground connected to the lower left pin, and +5 V connected to the upper right pin regardless of the total pin count. (eg., for a 16 pin DIP, ground is connected to pin 8 and +5 V is connected to pin 16)



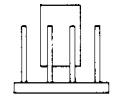
	+5V	GND
U2	8	16
U3	8	16
U4	8	16
U5	8	16
U6	8	16
U7	8	16
U500	8	16
U501	8	16
U502	8	16
U503	8	16
U504	8	16
U505	8	16
U506	8	16
U507	8	16



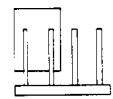
A60 J100



PLANE1 POSITION  
(Full Bright)

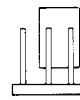


PLANE2 POSITION  
(Half Bright)

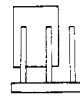


RUN POSITION

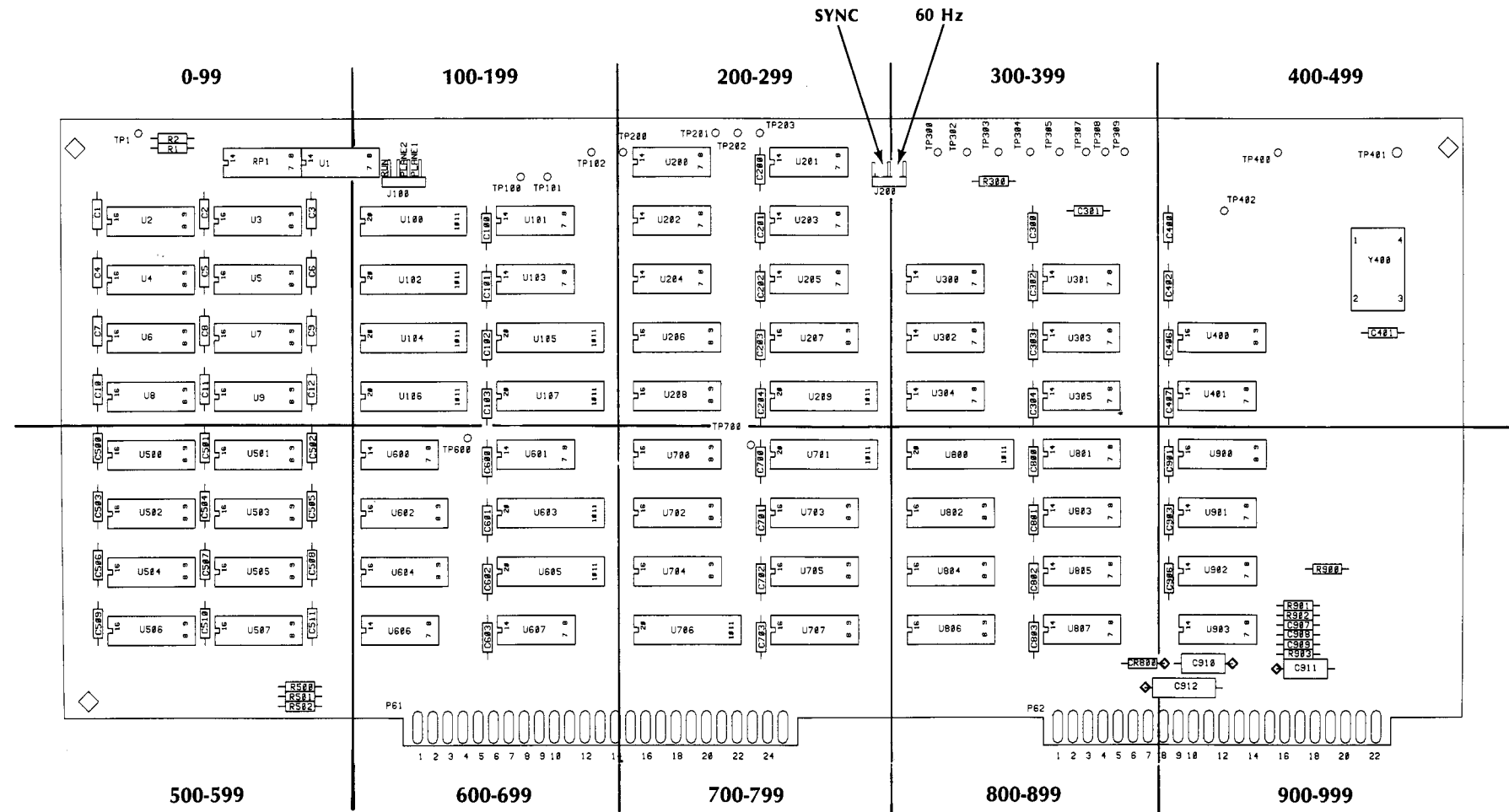
A60 J200

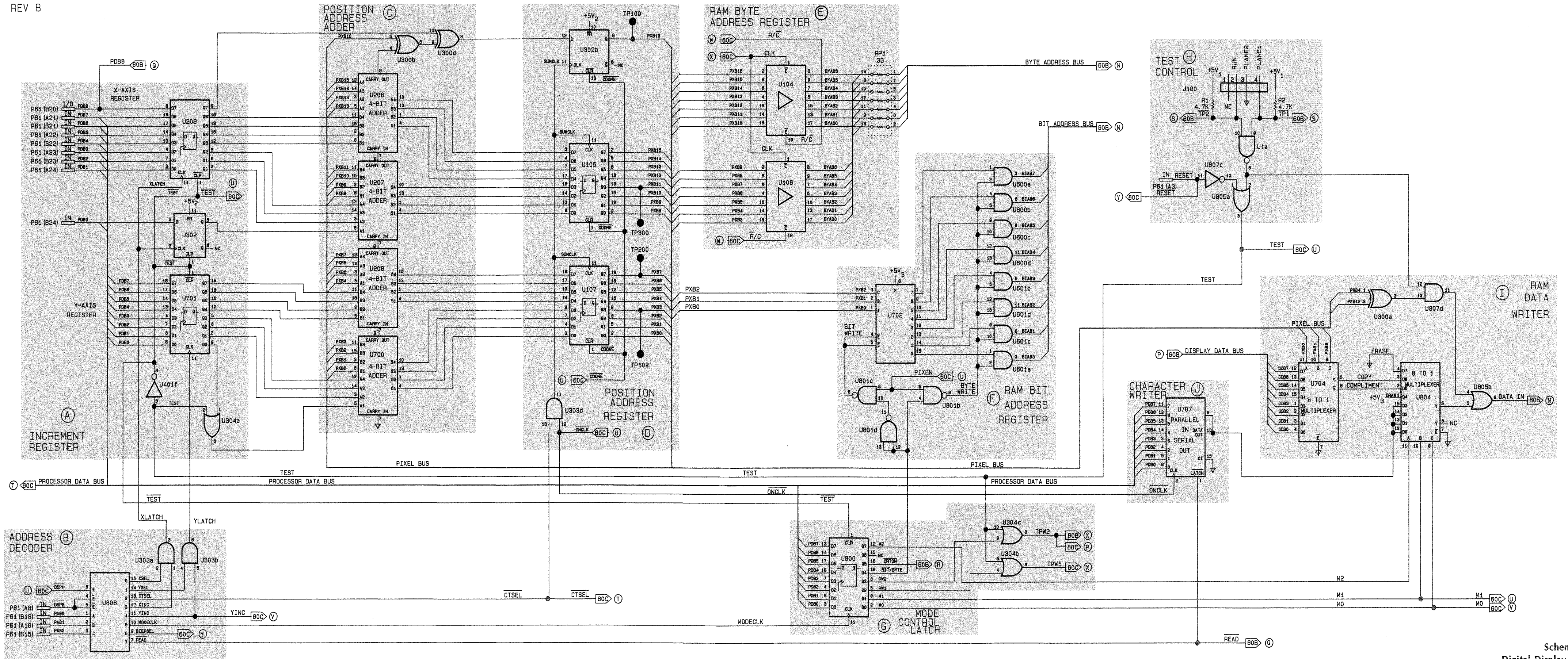


60 Hz Position

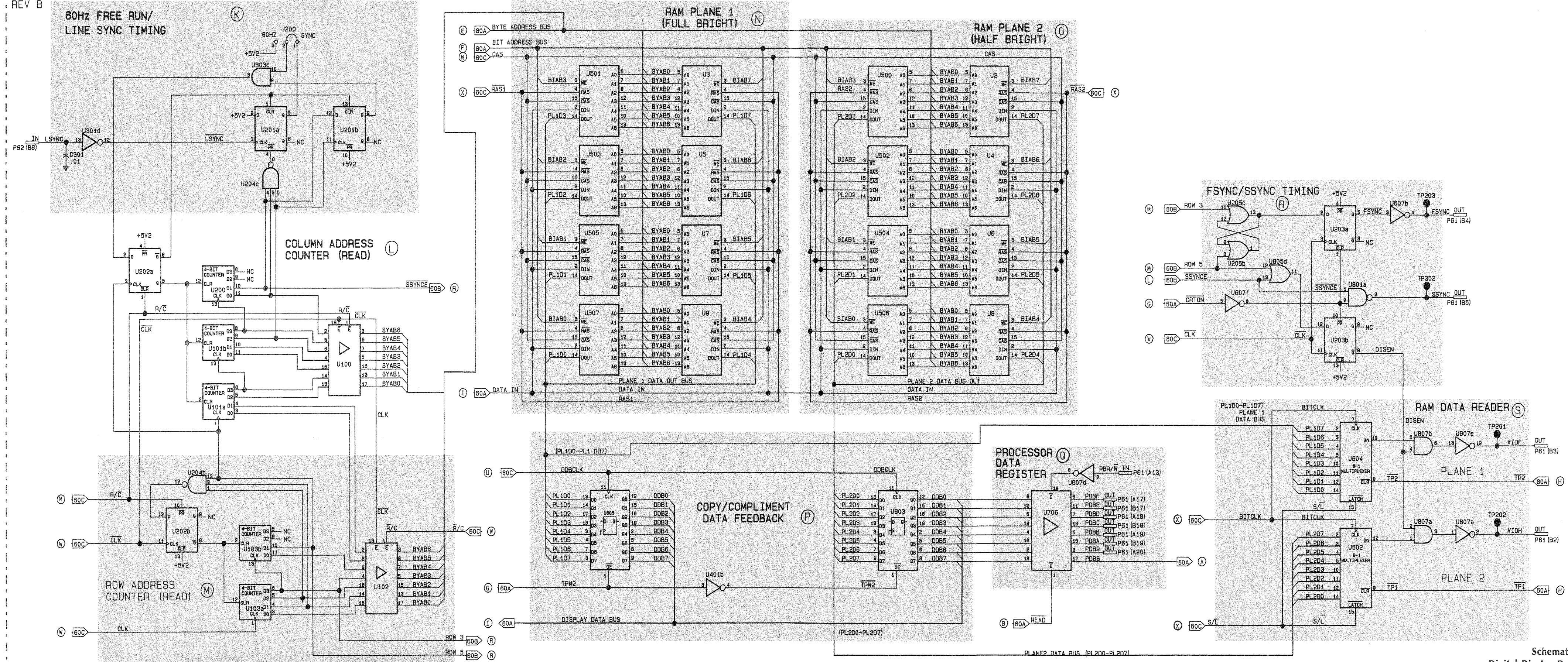


SYNC Position

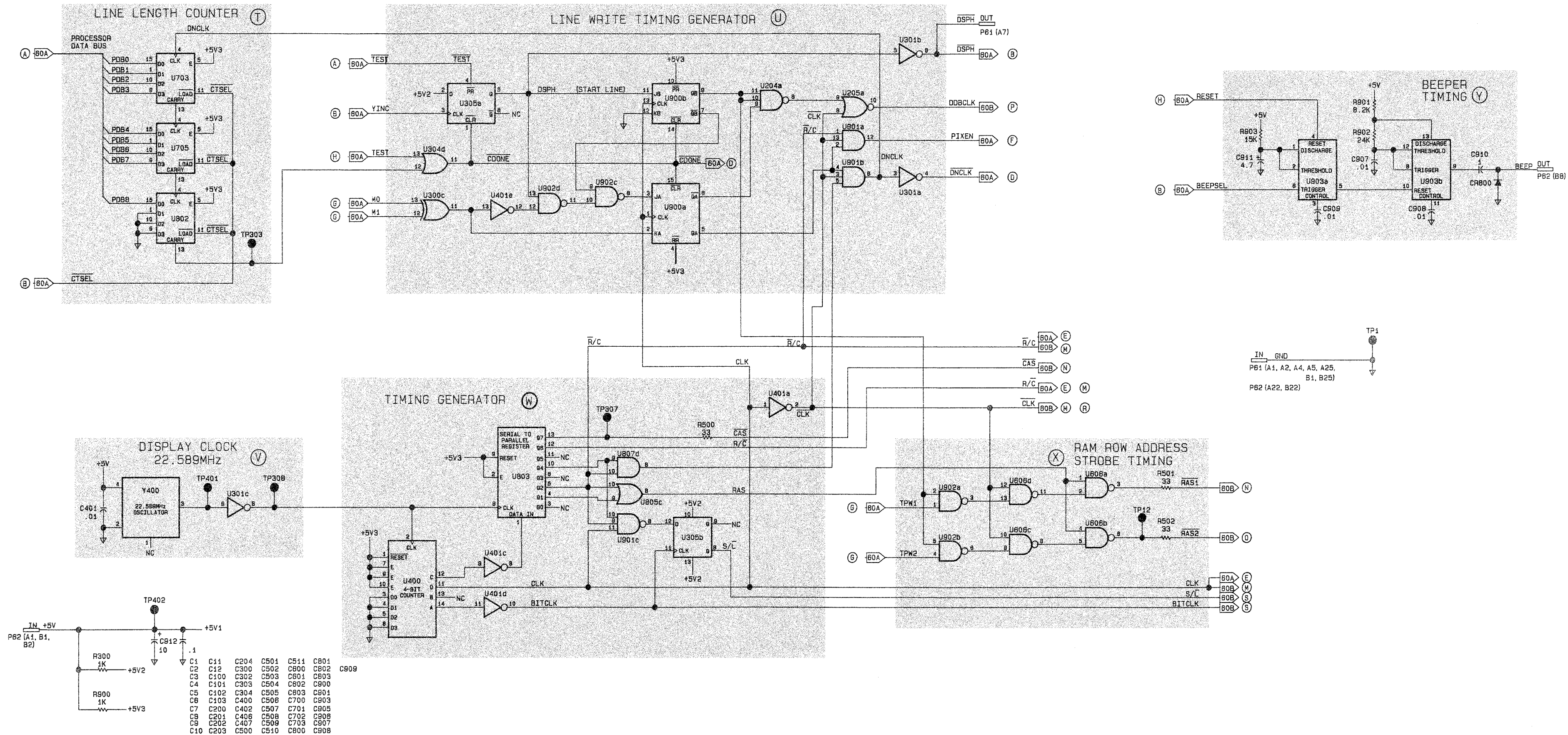












## **7-25 A65/A66 CMOS BUBBLE MEMORY ASSEMBLY**

### **7-26 Circuit Description: CMOS Bubble Memory**

#### **GENERAL**

The purpose of these assemblies is to store data in non-volatile memory. The A66 Assembly is standard and contains an 8k-byte CMOS RAM with battery backup. The optional A65 Assembly contains the same CMOS RAM with an additional 128k-byte Bubble memory module. The following information will concentrate on the optional A65 CMOS/Bubble Memory Assembly since it also contains the standard CMOS memory circuitry. The following theory will be to the circuit function level. Those circuits which are located on both the A65 and the A66 assemblies will be in (parenthesis). Table 7-53 identifies and describes the signals used on these assemblies.

#### **[A] BUBBLE ON/OFF**

When the Bubble Memory is addressed to read or write and the reset is not active, the Bubble On/Off circuit controls the Bubble Power Down circuit [H].

#### **[B] CONTROL SIGNAL BUFFER**

The Control Signal Buffer isolates the control signals which determine the read and write operation and whether the data is for the CMOS or the Bubble Memory.

#### **[C] (BUS DRIVERS)**

The Bus Drivers control the flow of data and address lines to and from the A65/66 Assemblies.

#### **[D] (CMOS MEMORY)**

This is the 8k-byte CMOS Memory and Page Select ICs. U203 selects which 256-bit page will be addressed.

#### **[E] BUBBLE INTERRUPT**

This circuit controls the interrupt from the Bubble Memory Controller circuit [I].

#### **[F] BUBBLE READ/WRITE**

This circuit controls the read and write operations of the Bubble Memory circuit by decoding the processor signals.

**[G] (BATTERY AND CMOS POWER DOWN)**

This circuit supplies either +5V or the battery to the CMOS IC to prevent data loss or corruption in the case of a power failure. When the instrument is turned on, +5V is supplied. When the instrument is turned off, the battery is smoothly switched in to prevent data loss.

**[H] BUBBLE POWER DOWN**

The Bubble Power Down holds the Bubble circuits in the power down state during the time that data transfer is not occurring. This method is used to prevent data loss or corruption in the case of a power failure.

**[I] BUBBLE CONTROLLER**

The Bubble Controller interfaces the Bubble circuits with the processor. It provides all the control and timing functions needed to operate the Bubble Circuitry.

**[J] BUBBLE COIL DRIVERS**

This circuit transforms the TTL inputs from the Bubble Controller [I] to high voltage drive signals. These drive signals then drive the coils internal to the Bubble Memory module U4. These coils generate the magnetic fields which move the bubbles within the module.

**[K] BUBBLE MEMORY**

There are three LSI devices in this circuit. They are as follows:

A Current Pulse Generator which contains individual current sinks that supply the proper currents when enabled by the respective TTL inputs.

A Sense Amplifier which reads and latches the bootloop from the Bubble Memory module. It then controls the address where data is to be read from or written to. This IC also contains an Error Correction circuit which detects and corrects data errors during both read and write operations.

The Magnetic Bubble Memory Module is a 128k-byte non-volatile solid state memory.

**[L] (CMOS CONTROL)**

This circuit controls the Battery and CMOS Power Down circuit [G] enabling it during a read or write operation and disabling it all other times.



**Table 7-53 Signal Descriptions**

<b>Signal</b>	<b>Description</b>
$\overline{\text{BUBS}}$	Bubble Select: Signal from the A40 Processor Assembly used enable the Bubble memory circuits to perform a read or write operation.
$\overline{\text{CMOSS}}$	CMOS Select: Signal from the A40 Processor Assembly used to clock data into the CMOS memory.
MAB0 through MABC	Memory Address Bus: These are the 12 Memory Address lines derived from the processor data bus lines 0-7 and processor address bus lines 0-4. They are used on this assembly only.
MDB0 through MDB7	Memory Data Bus: These are the 8 Memory Data Bus lines derived from the processor data bus. They are used on this assembly only.
PAB0 through PAB4	Processor Address Bus: These are five lines of the Processor Address Bus.
PAB5	Processor Address Bus: Bit 5 is used on this assembly to enable the CMOS Control circuit and Bubble Controller.
$\overline{\text{PBR/W}}$	Processor Bus Read/Write: This is the buffered processor R/W signal which programs the memory circuits to perform a read or write operation.
PDB0 through PDBF	Processor Data Bus: These are the 16 Processor Data bus lines.
4MHz	This clock is from the A40 Processor Assembly and is used by the A65/66 Assemblies as the main clock.

## 7-27 Troubleshooting The A65/66 Assemblies

### GENERAL

Failures in the CMOS/Bubble memory may or may not be detected by the power-up test routine. If the processor is not able to talk to the assembly, the processor will display "NONVOLATILE MEMORY ERROR: FORMAT REQUIRED" on the CRT display. If, however, there are memory location errors, error messages will be displayed during a store or recall operation.

If any of the following three failures occur on the optional Bubble Memory Assembly (03561-66565), the assembly will require formatting.

1. Replacement of the battery BT1
2. Replacement of IC U4.
3. Replacement of IC U103.

Format the assembly by pressing the following front panel keys:

```
PRESET
MODE .....TEST SELECT .....1 7 0 ENTER
START SNGL TST
```

The following built-in diagnostic routines can be used to determine if a failure exists in the CMOS or the Bubble portion and then to troubleshoot the defective circuit.

Test 19 CMOS Memory test which writes and reads a known pattern to the A66/A65 Assembly.

Test 20 Bubble Memory test which writes and reads a known pattern to the A65 Assembly.

Test 167 Bubble Memory Read DSA test used to troubleshoot the Bubble memory in the read mode.

Test 170 Memory Format Routine used to initialize the CMOS memory on the A65 Bubble Memory Assembly.

Two troubleshooting procedures are given. The first procedure is for the standard A66 CMOS Memory assembly. The second is for the optional A65 CMOS/Bubble Memory assembly.

**A66 CMOS TROUBLESHOOTING**



*Having the A66 cover removed exposes the power supply assemblies. These assemblies contain exposed ±170 primary voltage. Exercise extreme caution when troubleshooting since contact with these voltages can cause personal injury.*



*Always stop the diagnostic test routine from running before turning the instrument LINE power OFF! Otherwise, damage to the memory circuits will occur!*

Troubleshoot the circuits on the A66 Assembly in the order given in Table 7-54. In this table, level one circuits must be operational before level two circuits can be checked, etcetera. Test Routine 19, CMOS Memory Test, will be used to troubleshoot the A66 Assembly. To enter into self test routine 19, press the following -hp-3561A front panel keys in the order given:

```
PRESET
MODE ..... TEST SELECT ..... 19 ENTER
```

**Table 7-54 A66 Circuit Troubleshooting Order**

Level	Functional Blocks
1	Bus Drivers: C
2	CMOS Control: L
3	Battery And CMOS Power Down: G
4	CMOS Memory: D

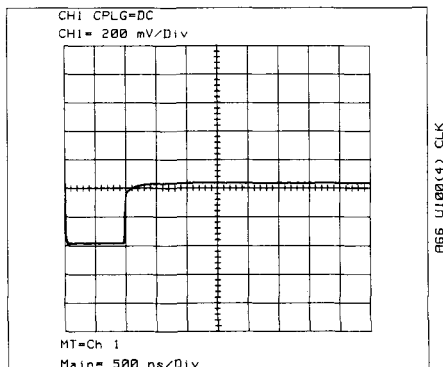
**[C] BUS DRIVERS**

With test routine 19 running continuously, check that the output pins of U101(3,5,7,9,12,14,16,18) are toggling. If any of the pins are not, replace U101.

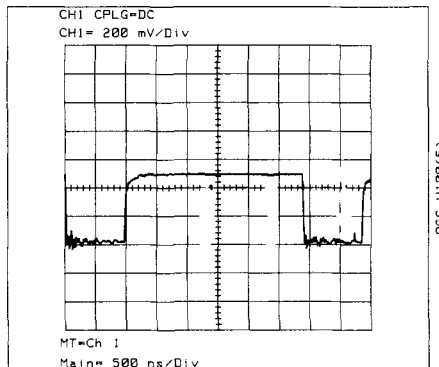
**[L] CMOS CONTROL**

With test routine 19 running continuously, verify the signals on the output of U100 with those shown in Figure 7-38. If either do not match, replace U100.

**Figure 7-38 Correct Waveforms At A66U100(4,5)**



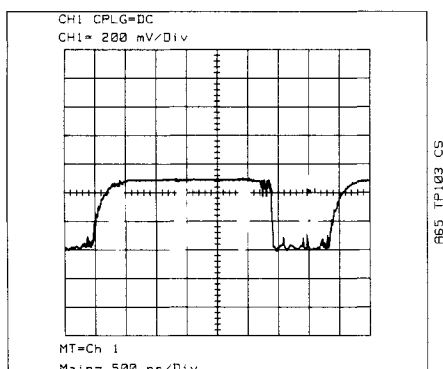
Probe: 10:1  
 Ch1: Connection- U100(4)  
 Coupling- dc  
 Ground- 3rd graticule from the bottom  
 Trigger: Int- Ch1  
 Slope- Negative



Probe: 10:1  
 Ch1: Connection- U100(5)  
 Coupling- dc  
 Ground- 3rd graticule from the bottom  
 Trigger: Int- Ch1  
 Slope- Negative

**[G] BATTERY AND CMOS POWER DOWN**

With test routine 19 running continuously, verify that TP102 is +5Vdc. Verify the signal at TP103 with that shown in Figure 7-39. Also, with test routine 19 stopped, turn the instrument power off and verify that the voltage on TP102 is greater than +2Vdc. If any measurements are incorrect, troubleshoot this functional circuit.

**Figure 7-39 Correct Waveform At A66 TP103**

Probe: 10:1

Ch1: Connection- TP103

Coupling- dc

Ground- 3rd graticule from the bottom

Trigger: Int- Ch1

Slope- Negative

**[D] CMOS MEMORY**

The troubleshooting for this circuit is to first replace U203. If the the failure remains, replace U103.

**A65 BUBBLE MEMORY TROUBLESHOOTING**

If at power-on, the CRT displays the message "NONVOLATILE MEMORY ERROR: FORMAT REQUIRED," perform the formatting routine by running Diagnostic Test Routine 170 located in Section VI. If after running this routine, the format message is still displayed, proceed with the following troubleshooting information.

**WARNING**

*Having the A65 cover removed exposes the power supply assemblies. These assemblies contain exposed  $\pm 170\text{Vdc}$  primary voltage. Exercise extreme caution when troubleshooting in this area since contact with these voltages can cause personal injury.*

**CAUTION**

*Always stop the test routine from running before turning the instrument LINE power OFF! Otherwise, damage to the memory circuits will occur!*

This troubleshooting procedure is for the Bubble Memory circuitry only. Troubleshooting information for the CMOS circuitry is given in Paragraph A66 CMOS Troubleshooting.

Use the failure isolation chart in Figure 7-40 to determine if the problem is in the Bubble or CMOS portion of the assembly.

Use the following flowchart to determine if the A65 failure is in the CMOS or Bubble portion of the circuitry. This flowchart will also determine if there is a hardware or a Bubble firmware failure (lost Seed or Bootloop).

All possible errors are listed in Table 7-55. Included in the list is the error number, a description of the failure and probable defective components or functional circuits which may have caused the error.

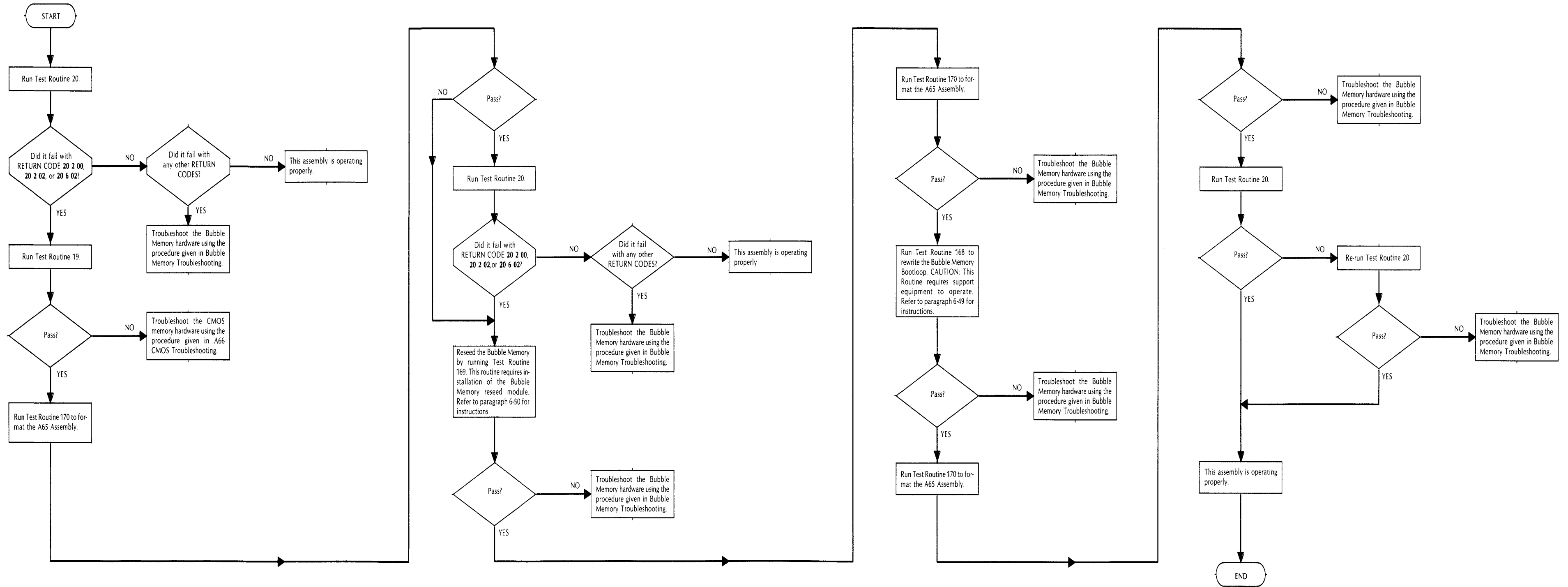


Figure 7-40 A65 Failure Isolation Chart

**Table 7-55 Test 20 RETURN CODE Descriptions**

<b>Error</b>	<b>Description</b>	<b>Probable Cause</b>
20 1 00	No Bubble is present or bad communication between the A40 Processor and A65 Bubble Memory Controller.	Usually caused by the Bus Driver U202. Verify its operation using the CMOS troubleshooting procedure.
20 2 00	The Bubble circuitry failed during a read operation.	Both errors 20 2 00 and 20 2 01 may be caused by either a defective Bubble module U4 or Current Pulse Generator U102. Verify using the K Bubble Memory troubleshooting procedure.
20 2 01	The Bubble circuitry failed during a write operation.	
20 2 02	Both errors 20 2 00 and 20 6 03 occurred.	
20 2 03	Both errors 20 2 01 and 20 6 03 occurred.	
20 6 00	The FIFO in the Controller U200 is failing.	Usually caused by the Bus Driver U202 and/or the Controller U200.
20 6 01	The Bootloop Register in the Sense Amplifier U3 is not communicating with the Controller U200.	Usually caused by a failure in the Sense Amplifier U3.
20 6 02	The Bubble cannot be initialized.	Usually caused by a failure in the CMOS Memory or the coil driver circuitry of the Bubble memory.
20 6 03	Data read from the Bubble Memory at initialization does not match the stored fixed pattern. The first time this test is performed, this failure will occur since the fixed pattern has not yet been written into memory. However, Test 20 writes and checks twice. If it fails the second time also, error 20 6 04 will occur.	Usually caused by a failure in the Bubble Coil Drivers J or the Bubble Memory K circuits.
20 6 04	Data pattern read from the Bubble memory does not match the stored fixed pattern. See also error 20 6 03.	
20 6 05	Both errors 20 2 00 and 20 2 01 occurred.	

The Bubble troubleshooting is performed with the -hp-3561A running in Test Routine 167. Troubleshoot the functional circuits in the order given in Table 7-56. In this table, level one circuits must be operational before level two circuits can be

checked, etcetera. To enter into Test Routine 167, press the following -hp-3561A front panel keys in the order given:

PRESET  
 MODE ..... TEST SELECT .....167 ENTER

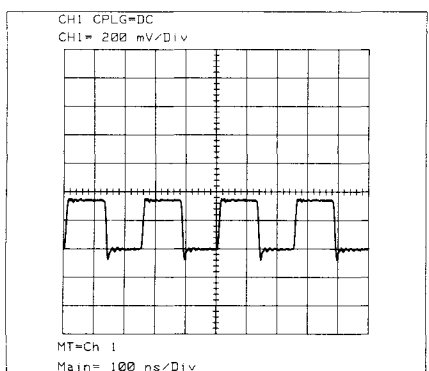
**Table 7-56 A65 Circuit Troubleshooting Order**

Level	Functional Blocks
1	Control Signal Buffer: B
2	Bubble On/Off: A
3	Bubble Power Down: H
4	Bubble Read/Write: F
5	Bus Drivers: C
6	Bubble Controller: I
7	Bubble Coil Drivers: J
8	Bubble Memory: K

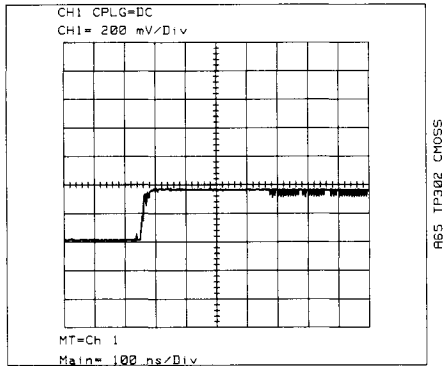
**[B] CONTROL SIGNAL BUFFER**

Verify that the outputs of U306(9,11,13) are toggling. Also check the waveforms at TP301 and TP302 with those shown in Figure 7-41. If any of these signals are not present, troubleshoot this functional block.

**Figure 7-41 Correct Waveforms At A65 TP301 And TP302.**



Probe: 10:1  
 Ch1: Connection- TP301  
 Coupling- dc  
 Ground- 3rd graticule from the bottom  
 Trigger: Int- Ch1  
 Slope- Positive

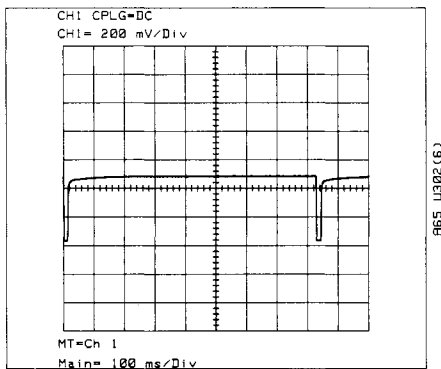


Probe: 10:1  
 Ch1: Connection- TP302  
 Coupling- dc  
 Ground- 3rd graticule from the bottom  
 Trigger: Int- Ch1  
 Slope-Negative

**[A] BUBBLE ON/OFF**

Verify the waveform at U302(6) with that shown in Figure 7-42. If it does not match, troubleshoot this functional block.

**Figure 7-42 Correct Waveform At A65 U302(6).**



Probe: 10:1  
 Ch1: Connection- U302(6)  
 Coupling- dc  
 Ground- 3rd graticule from the bottom  
 Trigger: Int- Ch1  
 Slope- Negative  
 BW Limit: On

**[H] BUBBLE POWER DOWN**

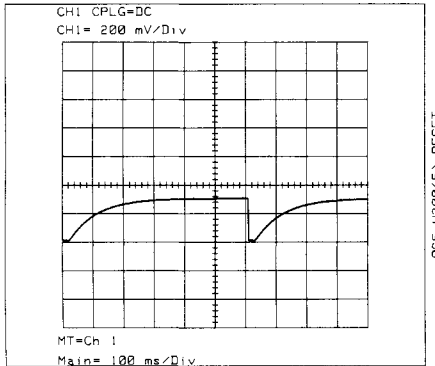
Verify the waveform at U300(5) with that shown in Figure 7-43. If it does not match, troubleshoot this functional block.

**[F] BUBBLE READ/WRITE**

Verify the waveforms at U201(8,11) with those shown in Figure 7-44. If they do not match, troubleshoot this functional block.



**Figure 7-43 Correct Waveform At A65 U300(5).**



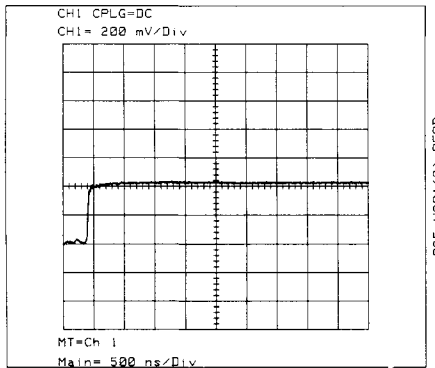
Probe: 10:1

Ch1: Connection- U300(5)  
Coupling- dc  
Ground- 3rd graticule from the bottom

Trigger: Int- Ch1  
Slope- Negative

BW Limit: On

**Figure 7-44 Correct Waveforms At A65 U201(8,11).**

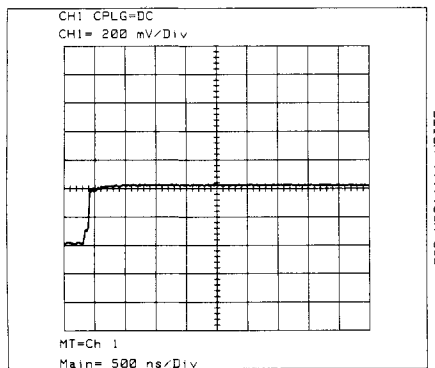


Probe: 10:1

Ch1: Connection- U201(8)  
Coupling- dc  
Ground- 3rd graticule from the bottom

Trigger: Int- Ch1  
Slope- Negative

BW Limit: On



Probe: 10:1

Ch1: Connection- U201(11)  
Coupling- dc  
Ground- 3rd graticule from the bottom

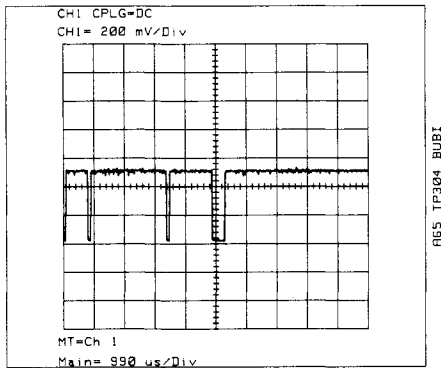
Trigger: Int- Ch1  
Slope- Negative

BW Limit: On

**[E] BUBBLE INTERRUPT**

Verify the waveform at TP304 with that shown in Figure 7-45. If it does not match, troubleshoot this functional block.

**Figure 7-45 Correct Waveform At TP304.**



Probe: 10:1

Ch1: Connection- TP304  
Coupling- dc  
Ground- 3rd graticule from the bottom

Trigger: Int- Ch1  
Slope- Negative

BW Limit: On

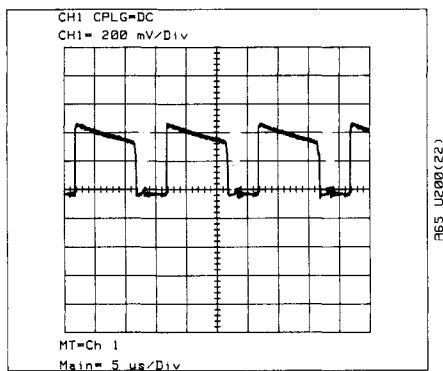
**[C] BUS DRIVERS**

Verify that all outputs of U202(2 through 9) are toggling. If any are not, replace U202.

**[I] BUBBLE CONTROLLER**

Verify the seven waveforms on the outputs of U200 with those shown in Figure 7-46. If any do not match, replace U200.

**Figure 7-46 Correct Output Waveforms At A65 U200.**



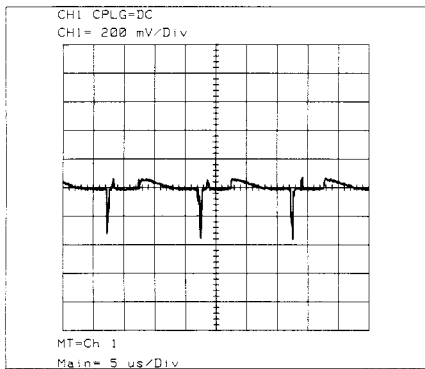
Probe: 10:1

Ch1: Connection- U200(22)  
Coupling- dc  
Ground- Center

Trigger: Int- Ch1  
Slope- Negative

BW Limit: Off

HF REJ: On



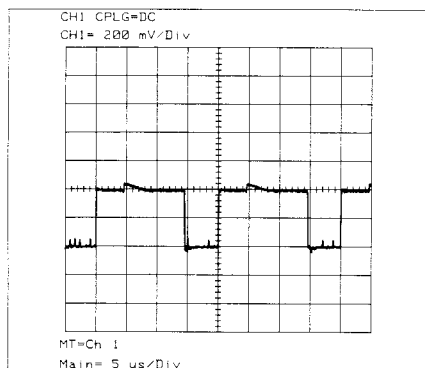
Probe: 10:1

Ch1: Connection- U200(23)  
Coupling- dc  
Ground- 3rd graticule from the bottom

Trigger: Int- Ch1  
Slope- Positive

BW Limit: Off

HF REJ: On

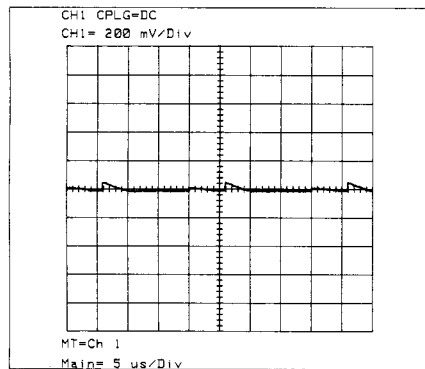


Probe: 10:1

Ch1: Connection- U200(24)  
Coupling- dc  
Ground- 3rd graticule from the bottom

Trigger: Int- Ch1  
Slope- Negative

BW Limit: On

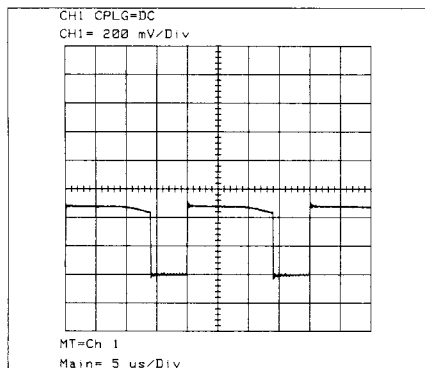


Probe: 10:1

Ch1: Connection- U200(30,31) or U102(6,9)  
Coupling- dc  
Ground- 3rd graticule from the bottom

Trigger: Int- Ch1  
Slope- Negative

BW Limit: Off

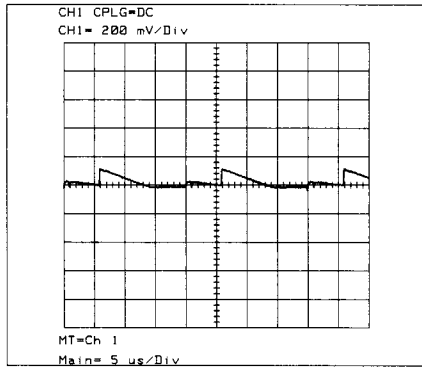


Probe: 10:1

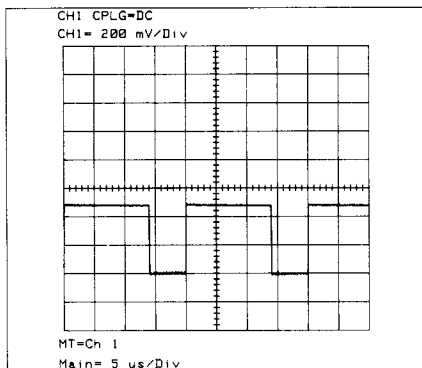
Ch1: Connection- U200(32,34) or U102(3,10)  
Coupling- dc  
Ground- 3rd graticule from the bottom

Trigger: Int- Ch1  
Slope- Positive

BW Limit: On



Probe: 10:1  
 Ch1: Connection- U200(33)  
 Coupling- dc  
 Ground- 3rd graticule from the bottom  
 Trigger: Int- Ch1  
 Slope- Negative  
 BW Limit: On



Probe: 10:1  
 Ch1: Connection- U200(36, 37, 38, 39) or  
 U2(3, 4, 5, 6)  
 Coupling- dc  
 Ground- 3rd graticule from the bottom  
 Trigger: Int- Ch1  
 Slope- Positive  
 BW Limit: On

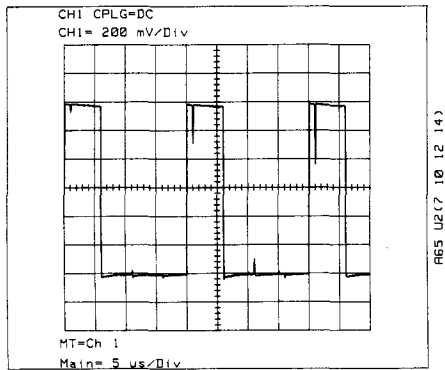
**[J] BUBBLE COIL DRIVERS**  
**[K] BUBBLE MEMORY**

Verify the waveforms on the outputs of U2(7, 9 through 15) with those shown in Figure 7-47. If any do not match, replace U2.

Verify the waveform on the outputs of U1 and U100 at test points TP1, TP2, TP4 and TP104 with those shown in Figure 7-48. If any do not match, replace the appropriate IC.

If the above waveforms are correct, replace U4.

**Figure 7-47 Correct Waveform At A65 U2.**

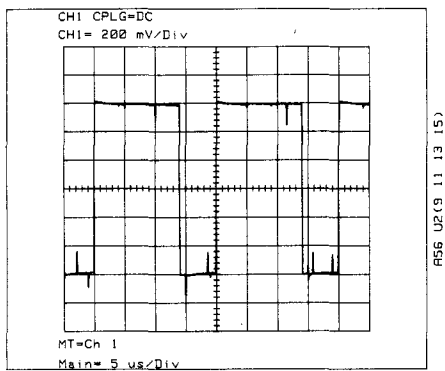


Probe: 10:1

Ch1: Connection- U2(7,10,12,14)  
Coupling- dc  
Ground- 2nd graticule from the bottom

Trigger: Int- Ch1  
Slope- Positive

BW Limit: On



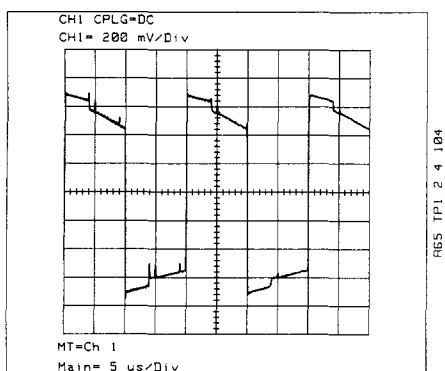
Probe: 10:1

Ch1: Connection- U2(9,11,13,15)  
Coupling- dc  
Ground- 2nd graticule from the bottom

Trigger: Int- Ch1  
Slope- Negative

BW Limit: On

**Figure 7-48 Correct Waveform At A65 U1 and U100 (TP1, 2, 4, 104).**



Probe: 10:1

Ch1: Connection- TP1, TP2, TP4, TP104  
Coupling- dc  
Ground- 2nd graticule from the bottom

Trigger: Int- Ch1  
Slope- Positive

BW Limit: On

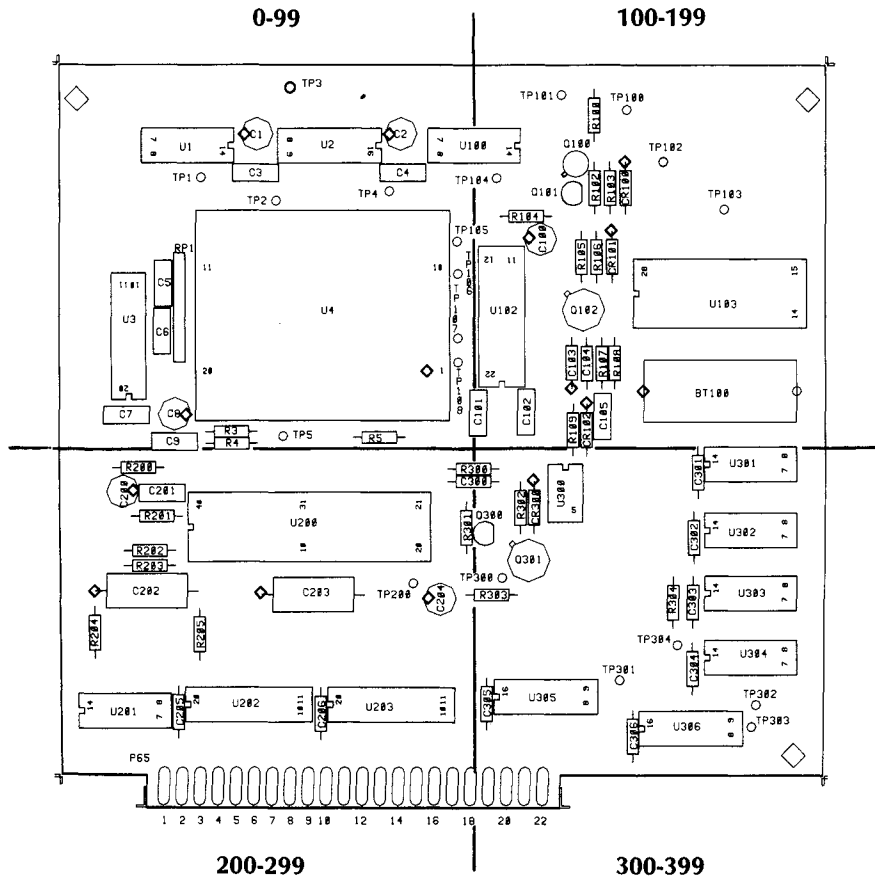
**Table 7-57 A66/65 Assembly Signal Connections**

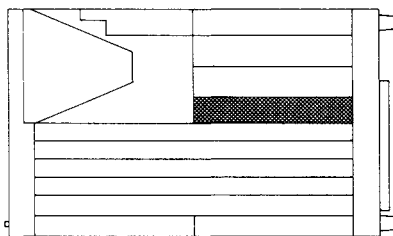
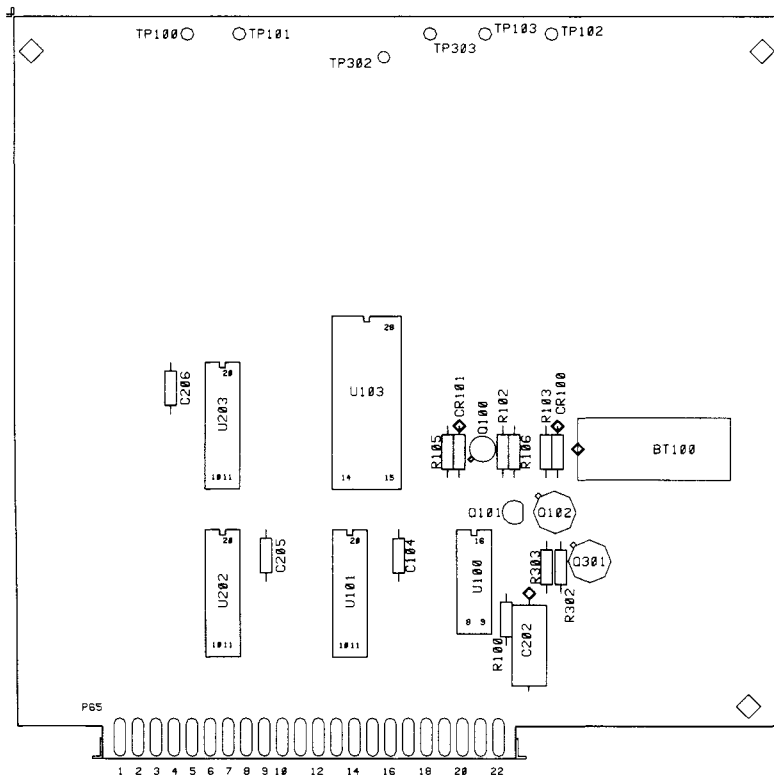
**INPUTS**

Signal Name	Functional Block	Connector Number	Origin Assembly
BUBS	B	P65(B16)	A40
CMOSS	B	P65(B18)	A40
PBR/W	B	P65(B15)	A40
RESET	A	P65(B17)	A40
Processor Address Bus	C	P65(A12 - A14)	A40
PAB0 - PAB5	C	P65(B12 - B14)	A40
PDB8	E	P65(A8)	A40
PDBF	A	P65(B11)	A40

**I/O SIGNALS**

Signal Name	Functional Block	Connector Number	Destination Assemblies
Processor Data Bus PDB0 - PDB7	C	P65(A4 - A7) P65(B4 - B7)	A30, A40, A50, A60, A80

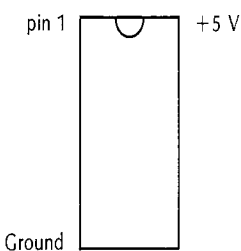




**A65 Assembly**

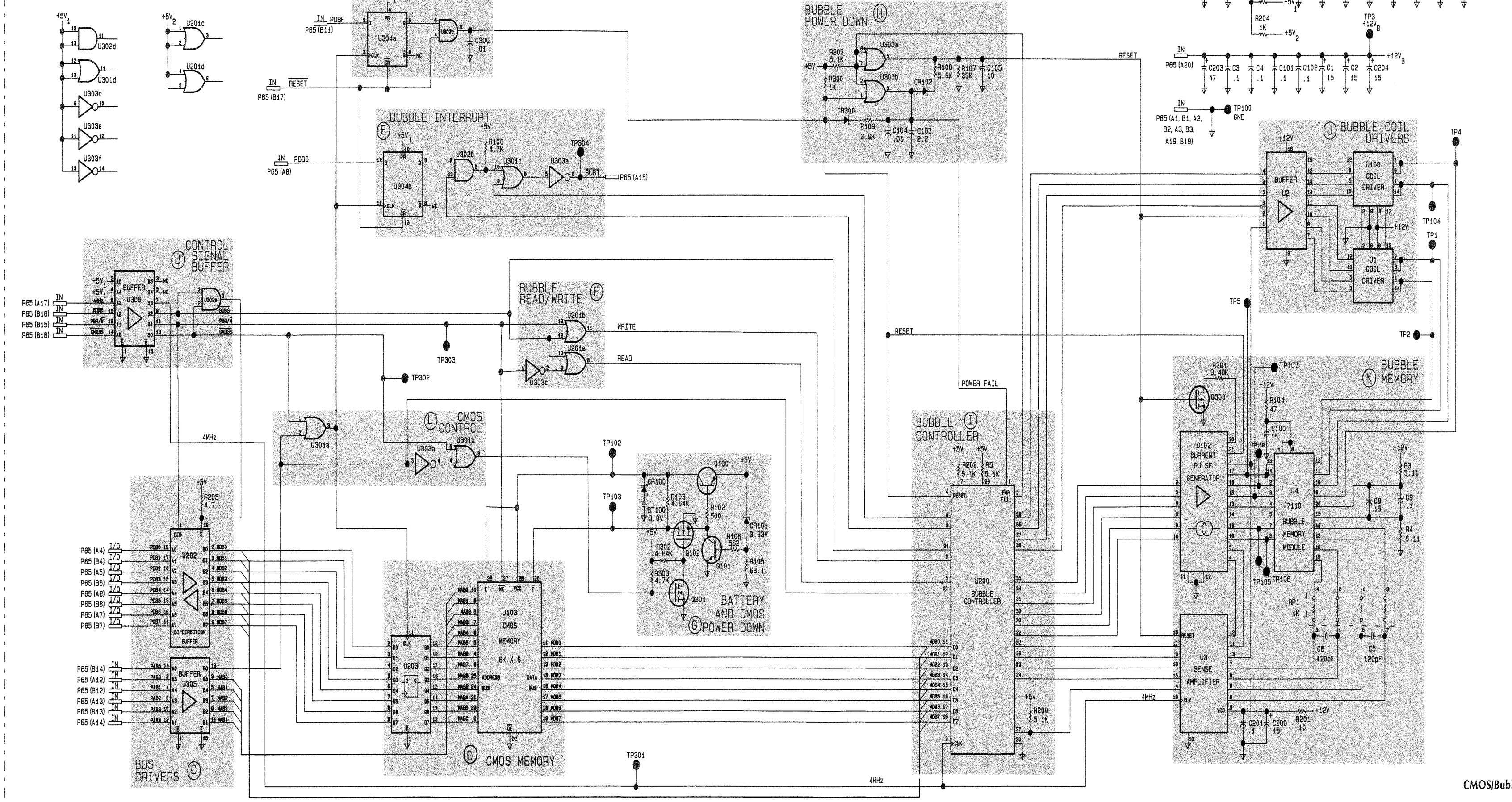
All integrated circuits are corner powered except those shown in the table below. Corner powered ICs have ground connected to the lower left pin, and +5 V connected to the upper right pin regardless of the total pin count. (eg., for a 16 pin DIP, ground is connected to pin 8 and +5 V is connected to pin 16)

Corner Power



	+12V	+5V	GND
U1	6,13		2,9
U2	16		8
U4	1,6		15
U100	6,13		2,9
U102	1	22	11,12
U103		28	22
U200		40	20

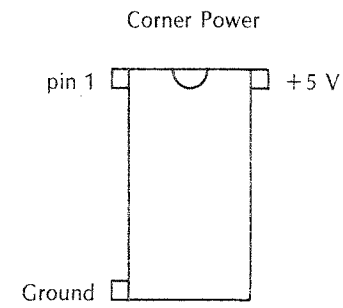
**A65 CMOS/BUBBLE MEMORY ASSEMBLY**  
03561-66565  
REV B





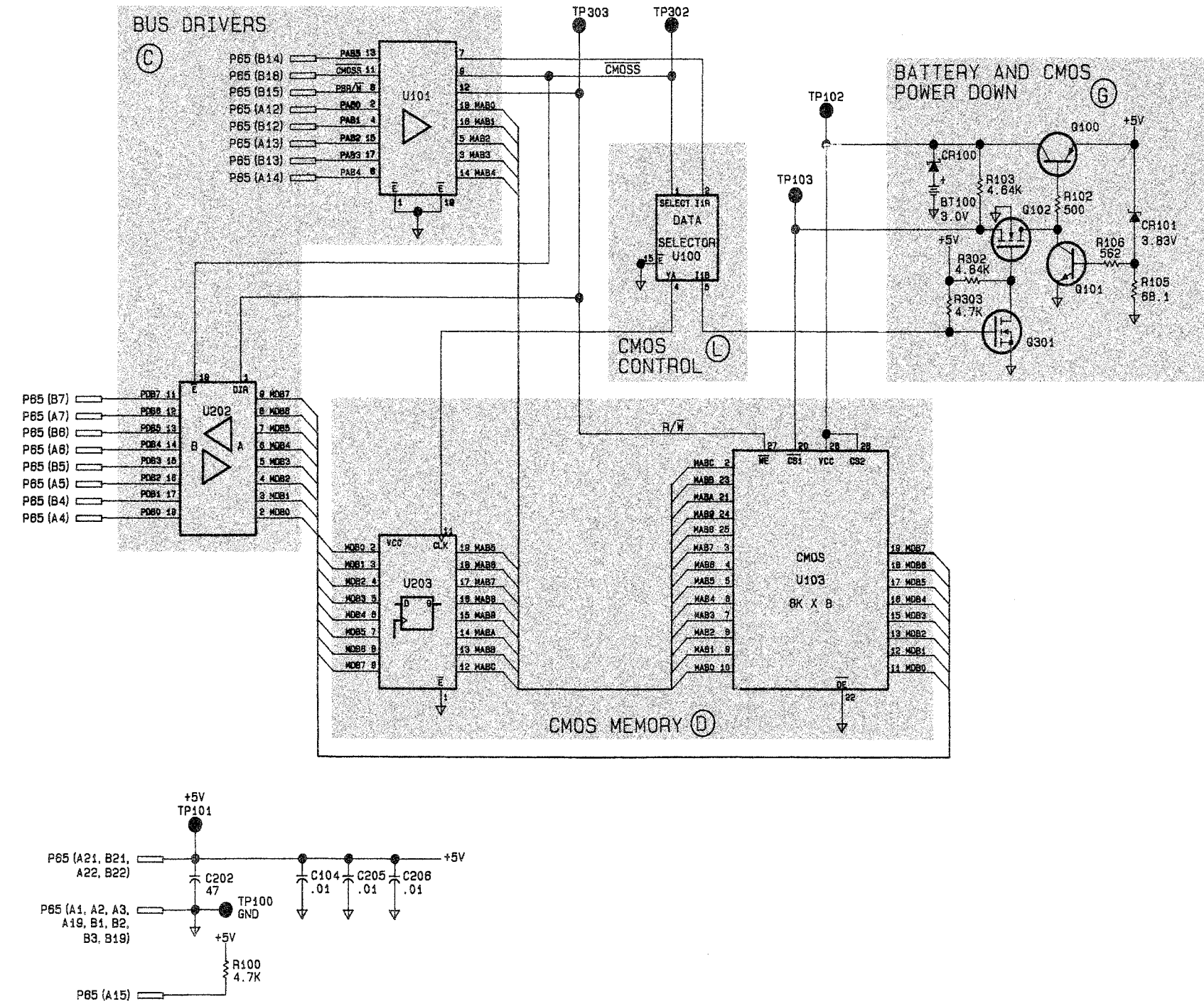
**A66 Assembly**

All integrated circuits are corner powered except those shown in the table below. Corner powered ICs have ground connected to the lower left pin, and +5 V connected to the upper right pin regardless of the total pin count. (eg., for a 16 pin DIP, ground is connected to pin 8 and +5 V is connected to pin 16)



	+5V	GND
U103	28	22

**A66** CMOS MEMORY ASSEMBLY  
03561-66566  
REV B



## **7-28 A70, A71, A72 POWER SUPPLY ASSEMBLIES AND PART OF A99 MOTHERBOARD ASSEMBLY**

### **7-29 Power Supply Circuit Description**

#### **GENERAL**

The -hp-3561A power supply is a Master/Slave switching supply. That is, one supply is used as the control (master) and the other supplies are "slaved" to the master. It uses two power MOS-FET transistors in a half-bridge configuration to drive the main power transformer at a frequency of 128 kHz. The duty-cycle of the drive is determined by the pulse-width control circuits which monitor the output of the master supply. The +5V master supply is used as the logic supply. Nine slave supplies, which are independently L-C filtered and post-regulated by 3-terminal regulators, are used by analog and isolated ground logic circuits.

There are two control feedback loops in the main +5V supply. A voltage feedback loop provides control of the supply output during normal operation. During an over-current condition, another loop takes control and provides current limiting.

The power supply has protection circuits which monitor the supply outputs. These circuits are connected to a latching fault supervisor circuit which turns off the gate drive of the power FETs. An LED is turned on when a fault is detected to indicate the fault condition. Any supply can cause a fault condition which would shut down all supplies.

A separate bias supply provides  $\pm 12V$  to the control circuits of the master supply. This supply uses 3-terminal linear regulators and derive its power from a separate power transformer. This supply must be present for operation of the power supply.

#### **[A] START UP CONTROL**

This circuit prevents the main supply from turning on until the bias supply voltage exceeds +11V. U101 compares the +5V reference voltage to a divided down +12V bias voltage. The output disables the "Over Current Sense Pulse Width Control" and "Fault Supervisor" circuits and sends the Start Up Enable signal to the SHUT input on the Pulse Width Modulator.

#### **[B] OVER CURRENT SENSE PULSE WIDTH CONTROL**

The over current control circuitry monitors the current through resistor R200. The voltage developed across R200 is input to comparator U401. As the current reaches maximum, U401 starts to turn Q1 and Q400 on. This causes the Pulse Width Modulator IC to reduce the duty-cycle of the switching FETs which reduces the supply current.

**[C] CLOCK SYNC CONTROL**

This circuit buffers the 256kHz clock from the A20 Assembly and drives the SYNC input of the Pulse Width Modulator. It also monitors the +5V main supply and inhibits the clock to the Pulse Width Modulator until the supply reaches 4.75 volts.

**[D] VOLTAGE SENSE PULSE WIDTH CONTROL**

This circuit compares the +5V main supply with the +5V reference. As the main supply starts to exceed the reference, this circuit pulls the COMP line lower causing the Pulse Width Modulator to reduce the duty-cycle of the drive to the switching FETs which reduces the main voltage.

**[E] PULSE WIDTH MODULATOR**

The Pulse Width Modulator is the controller for the -hp-3561A power supply. It drives the switching circuits in a manner which maintains a constant voltage at the supply output. It does this by varying the on-off time (duty cycle) of the switching FETs. The on-off time is controlled by the COMP input at U1(3). As this voltage level lowers, the on time becomes narrower.

**[F] SHUT DOWN DRIVER**

Signals from the Primary Current Sensor [K] and Fault Supervisor [L] are ORed at the input of the Shut Down Driver. Either of these two signals enable the Shut Down Driver to disable the Pulse Width Modulator IC and turn off the power supply.

**[G] POWER SUPPLY OVERVOLTAGE COMPARATORS****[H] ISOLATED POWER SUPPLY OVERVOLTAGE COMPARATORS**

These two circuits monitor the isolated and chassis-referenced supplies. If an overvoltage condition occurs in any one of the supplies, the overvoltage circuit will trigger the Fault Supervisor [L] and turn off the power supply.

**[I] VMOS DRIVER**

The VMOS Driver buffers the drive signals from the Pulse Width Modulator [E] and drives the switching FETs through transformer T200.

**[J] +5V OVERVOLTAGE COMPARATOR**

This circuit compares the +5V main supply with the +5V reference. If an overvoltage condition occurs, this circuit will activate the Fault Supervisor [L] to turn off the power supply.

**[K] PRIMARY CURRENT SENSOR**

Current transformer A70T600 senses the primary current of the main transformer A71T300. CR500, CR501 and U501c/d convert this current to a voltage at U501a/b pins 11 and 14. When a primary overcurrent condition is sensed, this circuit enables the Shut Down Driver [F] and turns off the power supply.

**[L] FAULT SUPERVISOR**

All fault-detecting-circuit outputs are latched by the Fault Supervisor. This latch turns off the Pulse Width Modulator through the Shut Down Driver [F] and lights a fault indicating LED during any fault condition. The four LEDs indicate which fault-detecting circuit was activated. These four LEDs are off during normal operation.

- CR1 — Primary Overcurrent Indicator
- CR2 — +5V Overvoltage Indicator
- CR3 — Power Supply Overvoltage Indicator  
(ground referenced slave supplies)
- CR4 — Isolated Power Supply Overvoltage Indicator  
(isolated slave supplies)

**[M] RECTIFIER/FILTER**

This Full-Wave bridge rectifier and R-C filter network convert the ac power input to approximately 170Vdc which is then supplied to the switching transistors [O]. When S2 is set to 115V, the Rectifier/Filter circuit functions as a voltage doubler. When S2 is set to 230V, the Rectifier/Filter circuit functions as a full-wave bridge.

**[N] BIAS TRANSFORMER**

The ac Line voltage is stepped down by the bias transformer and sent to the bias power supply circuitry [Q].

**[O] SWITCHERS**

The Switcher circuit consists of two switching power FETs and transient protection circuitry. The FETs are driven by the VMOS Driver [I] and switch the rectified line power to the power transformer.

**[P] LINE SYNC CONTROL**

The ac line signal taken from the secondary of the bias transformer is buffered and shaped by the Line Sync Control circuit. The sync output is used by the display circuitry as scan synchronization.

**[Q] BIAS VOLTAGE POWER SUPPLY**

The secondary voltage of the bias transformer is rectified and filtered to provide the  $\pm 12V$  bias supplies which are used by the various power supply control circuits.

**[R] LOW VOLTAGE DETECTOR**

This circuitry monitors the line voltage through the secondary of the bias transformer. If the line voltage drops below minimum level, this circuit sends a power fail signal to the A40 Processor Assembly.

**[S] +5V RECTIFIER**

This circuit rectifies and filters the +5V main supply. This supply powers the logic circuits.

**[T] INSTRUMENT GROUND RECTIFIERS**

This circuit rectifies one of the two multi-tap secondary windings of the power transformer to produce three supply voltages which are referenced to chassis ground.

**[U] ISOLATED GROUND RECTIFIERS**

This circuit rectifies one of the two multi-tap secondary windings of the power transformer to produce four supply voltages whose grounds are not referenced to the chassis (floating).

**[V] PS FILTER**

This is the L-C filtering circuitry for all slave supplies. The Zener diodes in this circuit provide overvoltage protection for the input of the three-pin regulators [W,X].

**[W] INSTRUMENT GROUND POWER SUPPLY**

These four linear regulators are on the A99 Motherboard Assembly. They provide the four regulated supplies which are chassis grounded.

**[X] ISOLATED GROUND POWER SUPPLY**

These five linear regulators are on the A99 Motherboard Assembly. They provide the five regulated supplies which are not referenced to chassis ground (floating ground).

## 7-30 Troubleshooting The Power Supply

**WARNING**

*The -hp-3561A Power Supply A70, A71 and A99 Assemblies contain exposed  $\pm 170$  primary voltages. Read the following safety consideration before attempting to troubleshoot the Power Supply assemblies. Contact with these voltages can cause serious personal injury.*

### SAFETY CONSIDERATION

The -hp-3561A power supply has many exposed areas which contain Primary voltage. These areas are shaded in red on the schematic and component locator. Extra care must be exercised when troubleshooting in these areas.

### GENERAL

The power supply in the -hp-3561A is a Master/Slave type. The troubleshooting procedure will be to determine:

- A. If the problem is in the Master or Slave power supply.
- B. Which functional circuit(s) of the power supply failed.

The power supply circuits between the A70, A71 and A72 Assemblies are interactive so the troubleshooting will be to isolate the problem to a functional circuit rather than to an assembly. The approach will be to verify which particular circuits are operating properly.

There are four LEDs on the A70 Assembly which are normally not lighted. When an LED is on, it indicates that a fault condition was detected and which monitoring circuit was involved. This will turn off the drive from the Pulse Width Modulator (shut down condition). However, the power supply can have a failure without an LED lit. For example, the Bias Supply can be bad which would not allow the power supply to operate, or there could be a low voltage condition which would not be detected by the power supply protect circuitry.

**WARNING**

*The heat sinks on the A70 Assembly are connected to  $\pm 170$  primary voltage. Exercise extreme caution when troubleshooting in this area. Contact with these voltages can cause serious personal injury.*

**WARNING**

*Wait at least three (3) minutes after power has been turned off before disconnecting the power supply cables W70 and W71, or removing the A70 or A71 Assemblies. A  $\pm 170$  Vdc charge is retained in the A99 Motherboard Assembly capacitors and a sudden discharge may occur if the wait-time is not observed.*

**REMOVING THE A20 ASSEMBLY**

In normal operation, the A20 Assembly provides the 256 kHz switching clock to the power supply. However, when the A20 Assembly is removed the power supply pulse width modulation circuit will generate its own clock. To prevent the A20 Assembly Clock from interfering with power supply troubleshooting, remove the A20 Assembly before troubleshooting any part of the power supply.

**ISOLATING THE PROBLEM TO THE MASTER OR SLAVE SUPPLY****CAUTION**

*When removing or inserting any PC Assembly, the ac Line switch must be in the OFF position. Otherwise, PC Assembly damage may occur.*

There are four protection circuits which will light the LEDs on the A70 Assembly. They are primary overcurrent, +5V master overvoltage, power supply overvoltage and isolated power supply overvoltage. If any of these LEDs are on and the power supply is shut down, turn the main power off and remove the A72 Assembly. Turn the main power on. If none of the LEDs light, the master +5V supply is working and the problem is in the slave supply. Troubleshoot the slave supply.

If any of the LEDs light, and the power supply is shut down, turn the main power off and disconnect W71 from A70J300. This will disable the main power transformer and rectifiers. Turn the main power switch on. If any of the LEDs light, there is a problem in the protection circuitry. Troubleshoot the protection circuits.

If none of the LEDs light, there is a problem in the main power transformer (A71T300) or the rectifier circuits [S],[T], or [U] blocks on the power supply schematic.

**TROUBLESHOOTING THE SLAVE SUPPLY**

Isolate the problem to one or more of the slave supplies by lifting one of the legs of the input inductors on the A72 Assembly (PS Filter block [V]). Troubleshoot the faulty slave supply. Note that switching the front panel input reference switch to CHASSIS connects the isolated ground to the chassis.

## TROUBLESHOOTING THE MASTER SUPPLY

There are three supplies needed in order for the master supply to operate. They are the  $\pm 12\text{V}$  Bias and the  $+5\text{V}$  reference. The Bias supply circuitry is on the A71 Assembly [Q], with its transformer on the A99 Assembly. The  $+5\text{V}$  reference is generated by the PWM IC U1(18) on the A70 Assembly. Also needed is the Sync signal coming into the PWM IC at U1(12). Before troubleshooting the master supply, verify that the bias and reference supplies and sync signal are operating.

### WARNING

*This setup procedure exposes  $\pm 170\text{Vdc}$  primary voltage on the large heat sinks and other parts of the A70 Assembly. Extreme caution must be exercised when troubleshooting during this condition. Contact with the high voltage can cause serious personal injury.*

## A70 [G],[H],[J],[K],[L] TROUBLESHOOTING

Place the A70 Assembly on an extender board and remove cable W70 from A70J700 (to the A99 Motherboard Assembly). This removes the  $\pm 170\text{Vdc}$  primary voltage from the A70 and A71 Assemblies. Turn on the AC Line power switch. If one of the A70 LEDs comes on and the main power supply is shut down, there may be problem in the protection circuit. Troubleshoot the indicated protection circuit.

## A70 [B],[D] TROUBLESHOOTING

With the cable removed from A70J700, turn on the main power switch. If no LEDs light, and the main supply is shut down, the problem may be in the pulse-width feedback control or the primary switching circuits. To verify proper operation of the feedback pulse-width control circuits [B] and [D]:

1. Adjust a dc power supply to  $5\text{V} \pm .2\text{V}$  and connect it to A70TP105 (+ to TP105, - to TP130).
2. Monitor the pulse width signal at A70TP100 and A70TP101.
3. Increase the dc supply voltage to  $+6\text{V}$ . The pulse width should change width to minimum. If it does not, troubleshoot the Voltage Sense Pulse Width Control circuit [D].
4. Monitor the pulse width at A70TP100 and TP101 (drive signal).
5. Connect a clip lead to TP400. Ground the other end of the clip lead. The pulse width should change width to minimum. If it does not, troubleshoot the Over-current Sense Pulse Width Control [B].

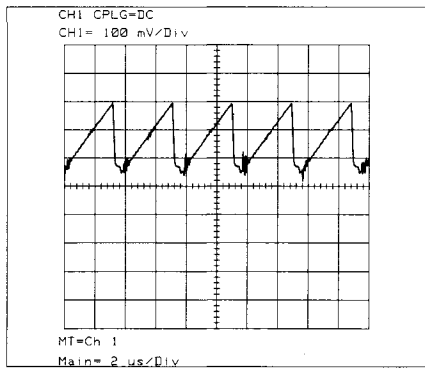
If these two pulse width control circuits are working, troubleshoot the primary switching circuits [O] and [I].



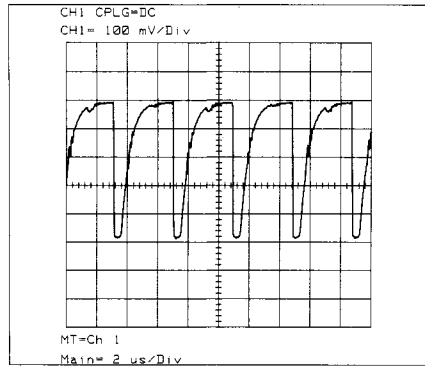
**OSCILLOSCOPE SIGNAL PICTURES**

The oscilloscope plots are used for troubleshooting the power supply. Note that all measurements are taken with a 10:1 probe. Other notes unique to the measurement are written next to the plot. Figure 7-49 gives those waveforms necessary for troubleshooting circuits on the A70 Assembly and Figure 7-50 gives those waveforms necessary for troubleshooting circuits on the A71 Assembly.

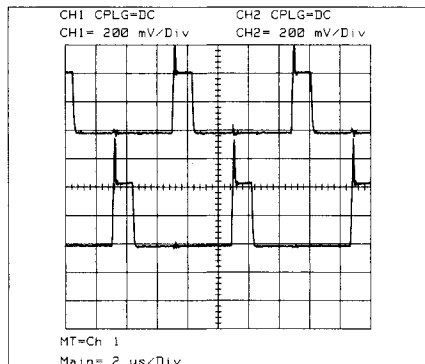
**Figure 7-49 A70 Assembly Troubleshooting Waveforms**



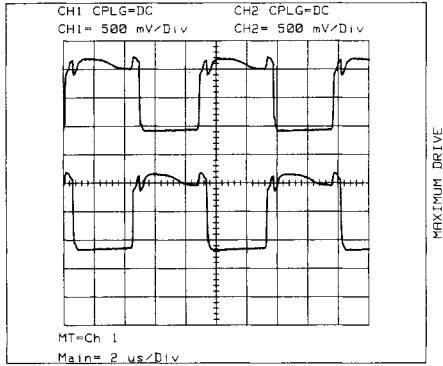
Probe: 10:1  
 Ch1: Connection- A70U1(10)  
 Coupling- dc  
 Ground- Center Graticule  
 Trigger: Internal-Ch1  
 Slope: Positive  
 Bandwidth Limit: On



Probe: 10:1  
 Ch1: Connection- A70U1(12)  
 Coupling- dc  
 Ground- Third Graticule From Bottom  
 Trigger: Internal-Ch1  
 Slope: Positive  
 Bandwidth Limit: On



Probe: 10:1  
 Ch1: Connection- A70U100(10)  
 Coupling- dc  
 Ground- Third Graticule From Top  
 Ch2: Connection- A70U100(5)  
 Coupling- dc  
 Ground- Third Graticule From Bottom  
 Trigger: Internal-Ch1  
 Slope: Positive  
 Bandwidth Limit: On



Probe: 10:1

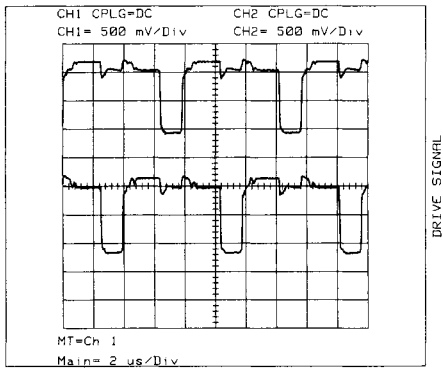
Ch1: Connection- A70 TP100  
Coupling- dc  
Ground- Third Graticule From Top

Ch2: Connection- A70 TP101  
Coupling- dc  
Ground- Third Graticule From Bottom

Trigger: Internal-Ch1  
Slope: Positive

Bandwidth Limit: On

This is the drive signal at maximum duty cycle (cable removed from A70J700)



Probe: 10:1

Ch1: Connection- A70 TP100  
Coupling- dc  
Ground- Third Graticule From Top

Ch2: Connection- A70 TP101  
Coupling- dc  
Ground- Third Graticule From Bottom

Trigger: Internal- Ch1  
Slope: Positive

Bandwidth Limit: On

This is the drive signal at normal duty cycle (all assemblies installed).



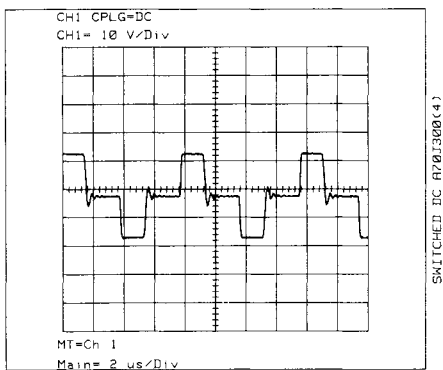
**WARNING! THIS MEASUREMENT CONTACTS 300VP-P PRIMARY DC VOLTAGE. USE EXTREME CAUTION WHEN PROBING THIS SIGNAL!**

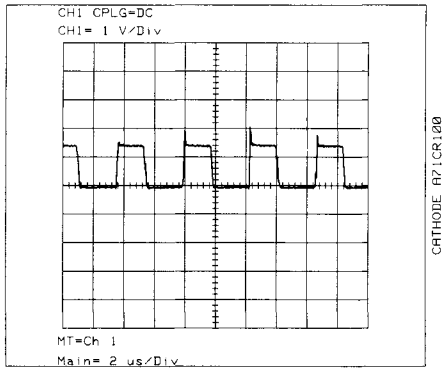
Probe: 10:1, 10M $\Omega$ , 600V Maximum Voltage (-hp-10014A)

Ch1: Connection- A70J300(4)  
Coupling- dc  
Ground- Center Graticule

Trigger: Internal-Ch1  
Slope: Positive

Bandwidth Limit: On





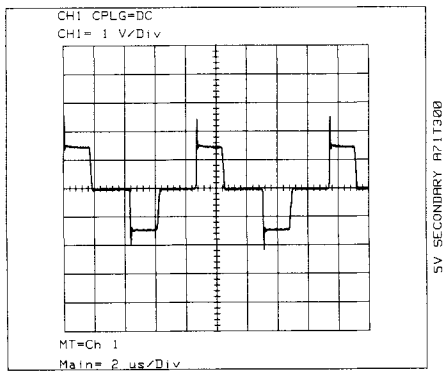
Probe: 10:1

Ch1: Connection- Cathode of A70CR100  
Coupling- dc  
Ground- Center Graticule

Trigger: Internal-Ch1  
Slope: Positive

Bandwidth Limit: On

Figure 7-50 Correct Waveform At A71CR100

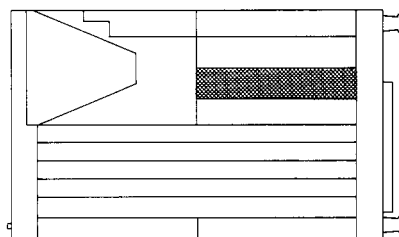
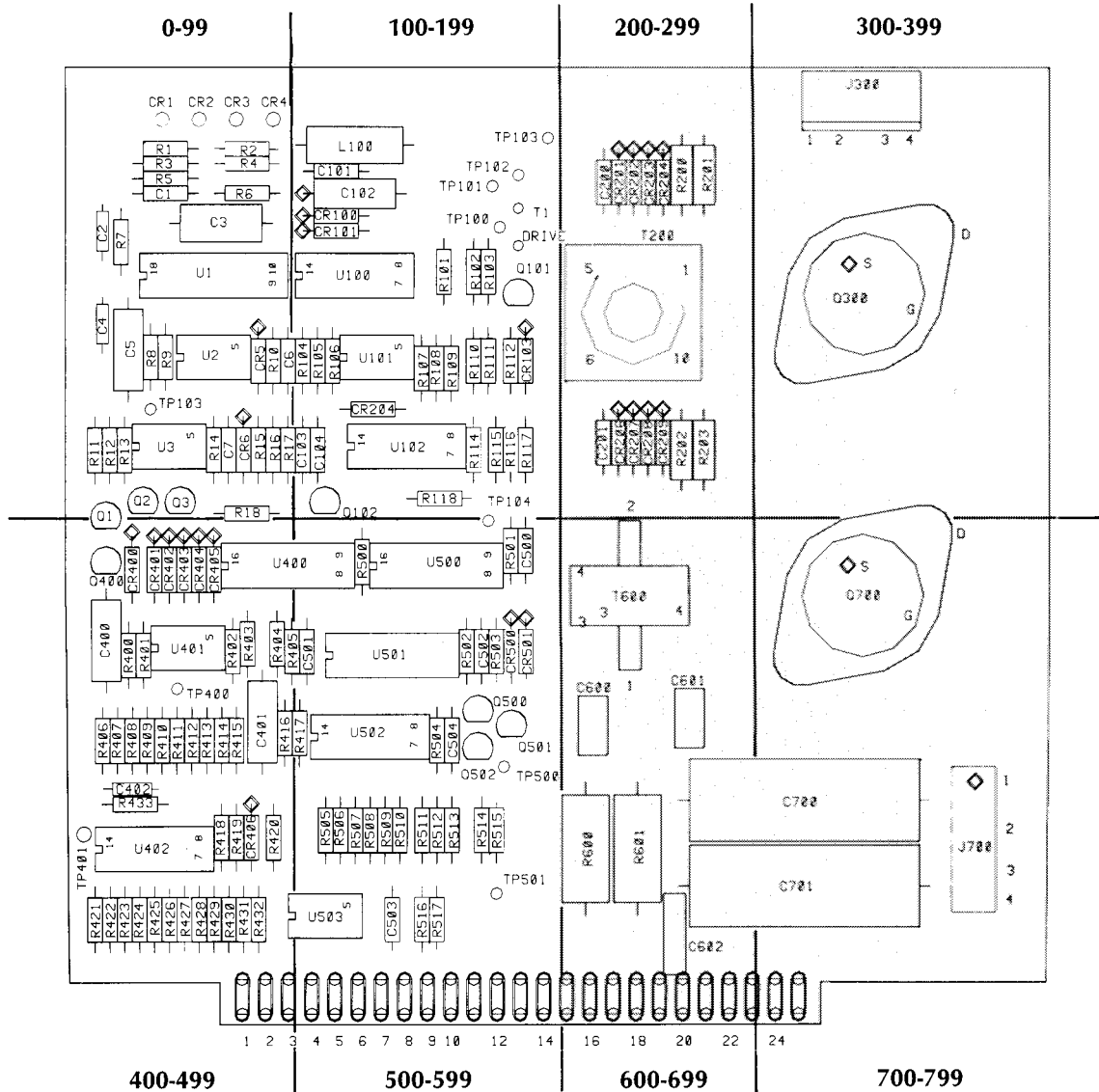


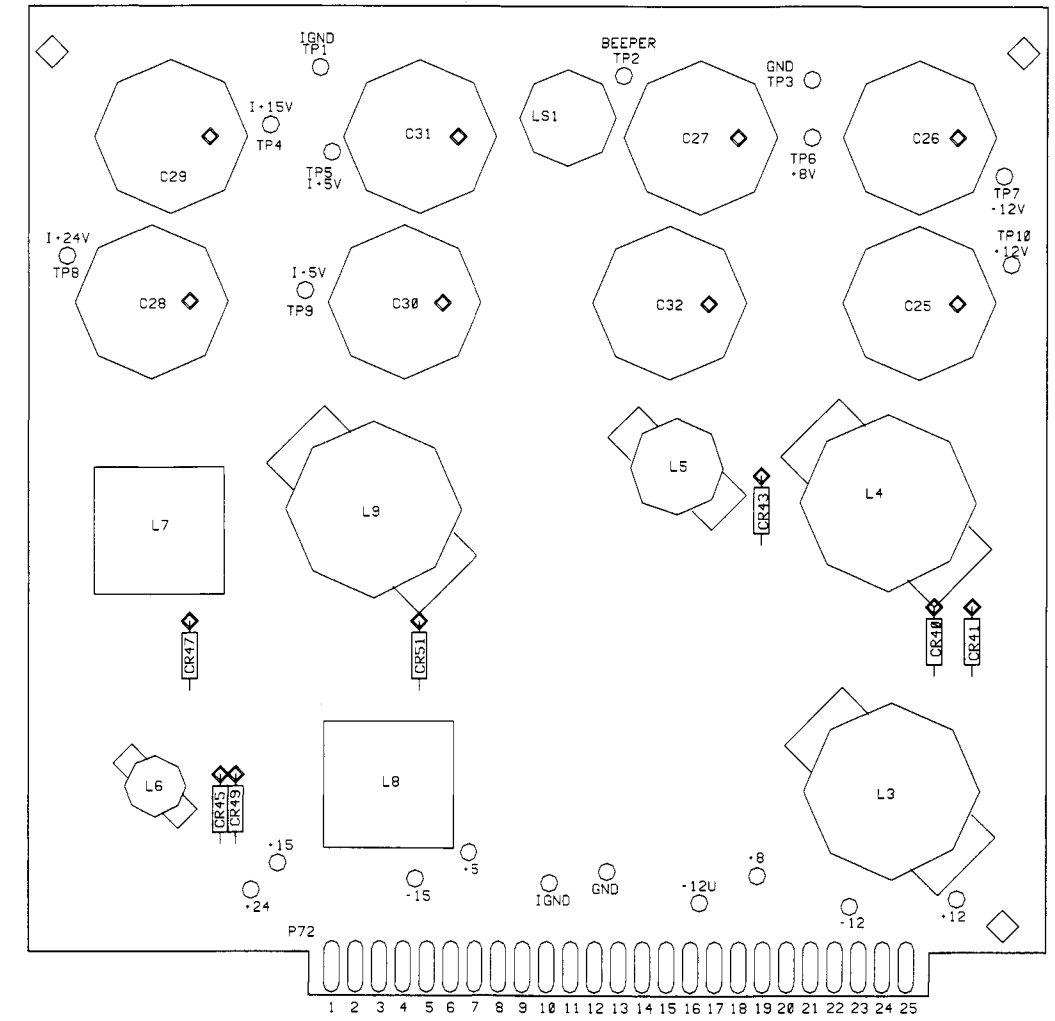
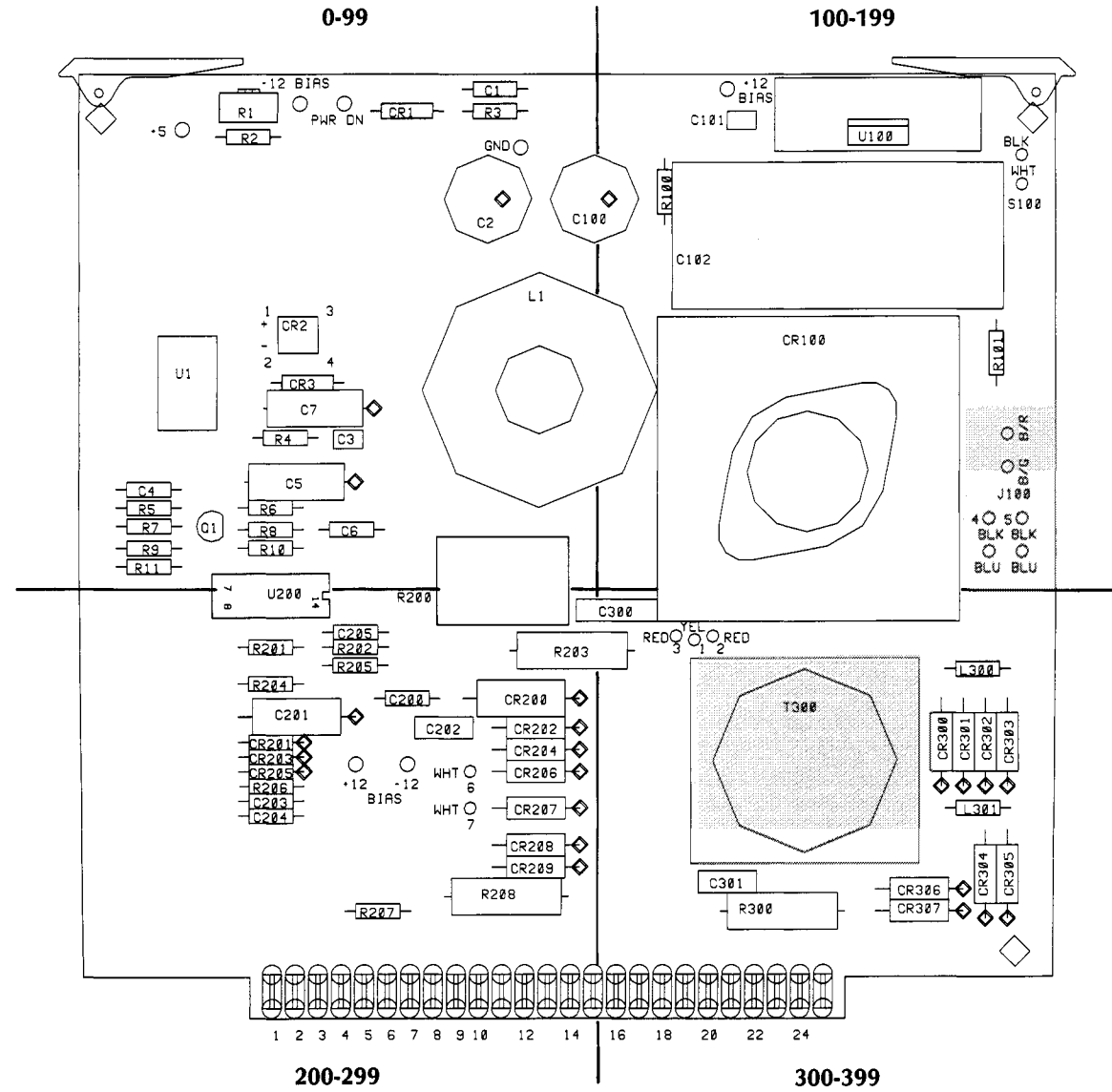
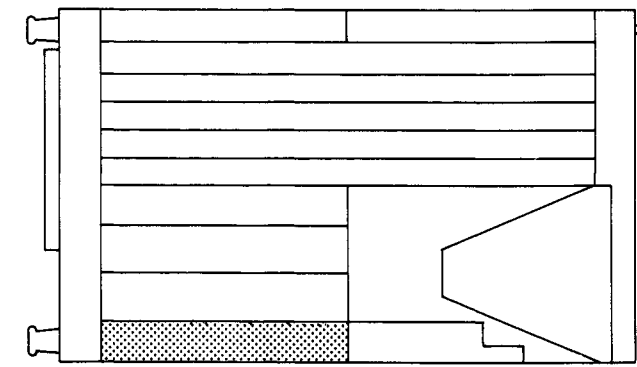
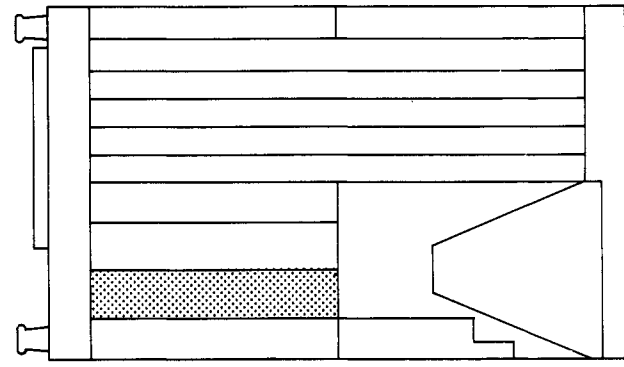
Probe: 10:1

Ch1: Connection- Junction Of A71CR100  
and A71R203  
Coupling- dc  
Ground- Center Graticule

Trigger: Internal-Ch1  
Slope: Positive

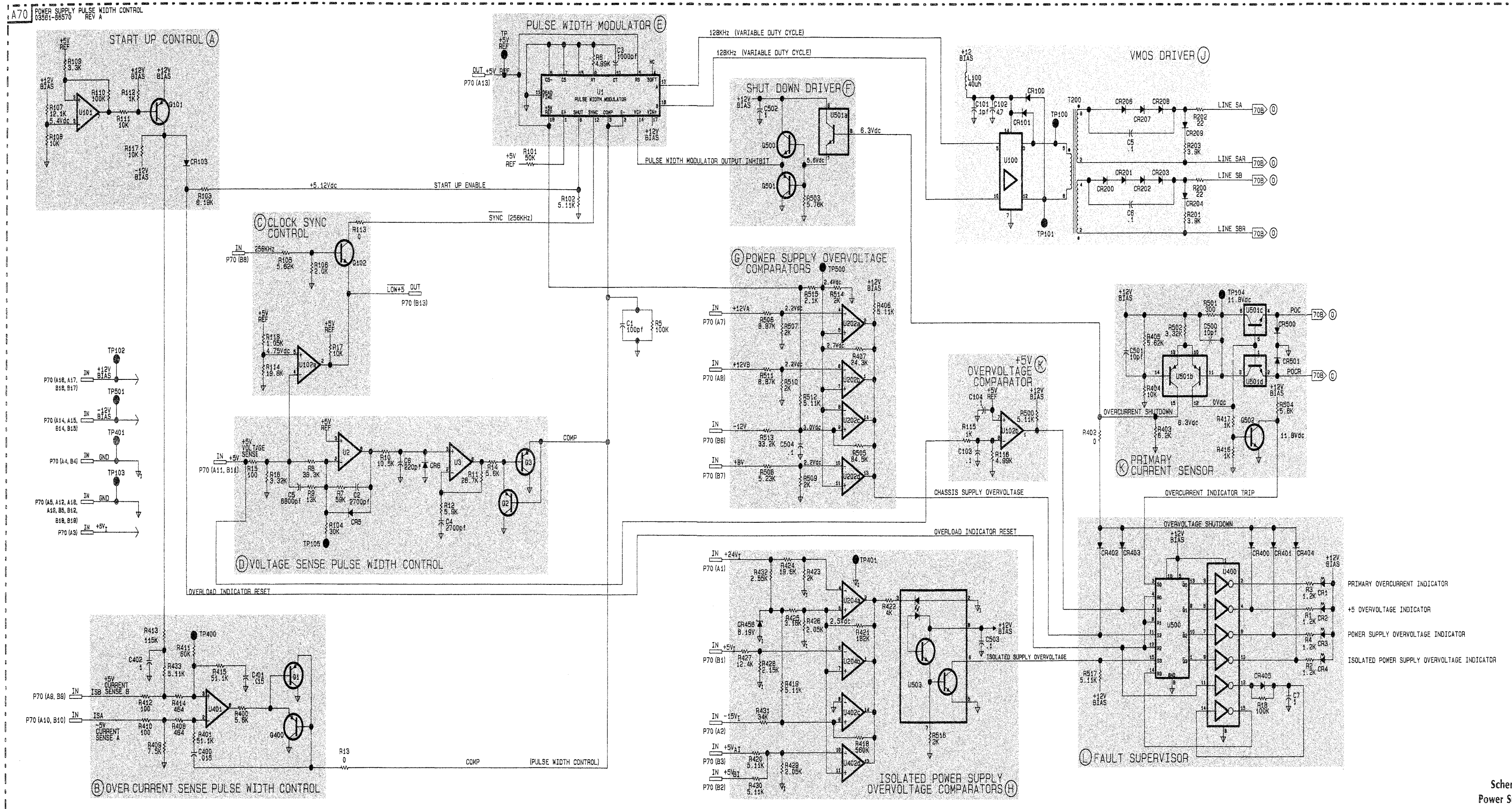
Bandwidth Limit: On





A70 Assembly

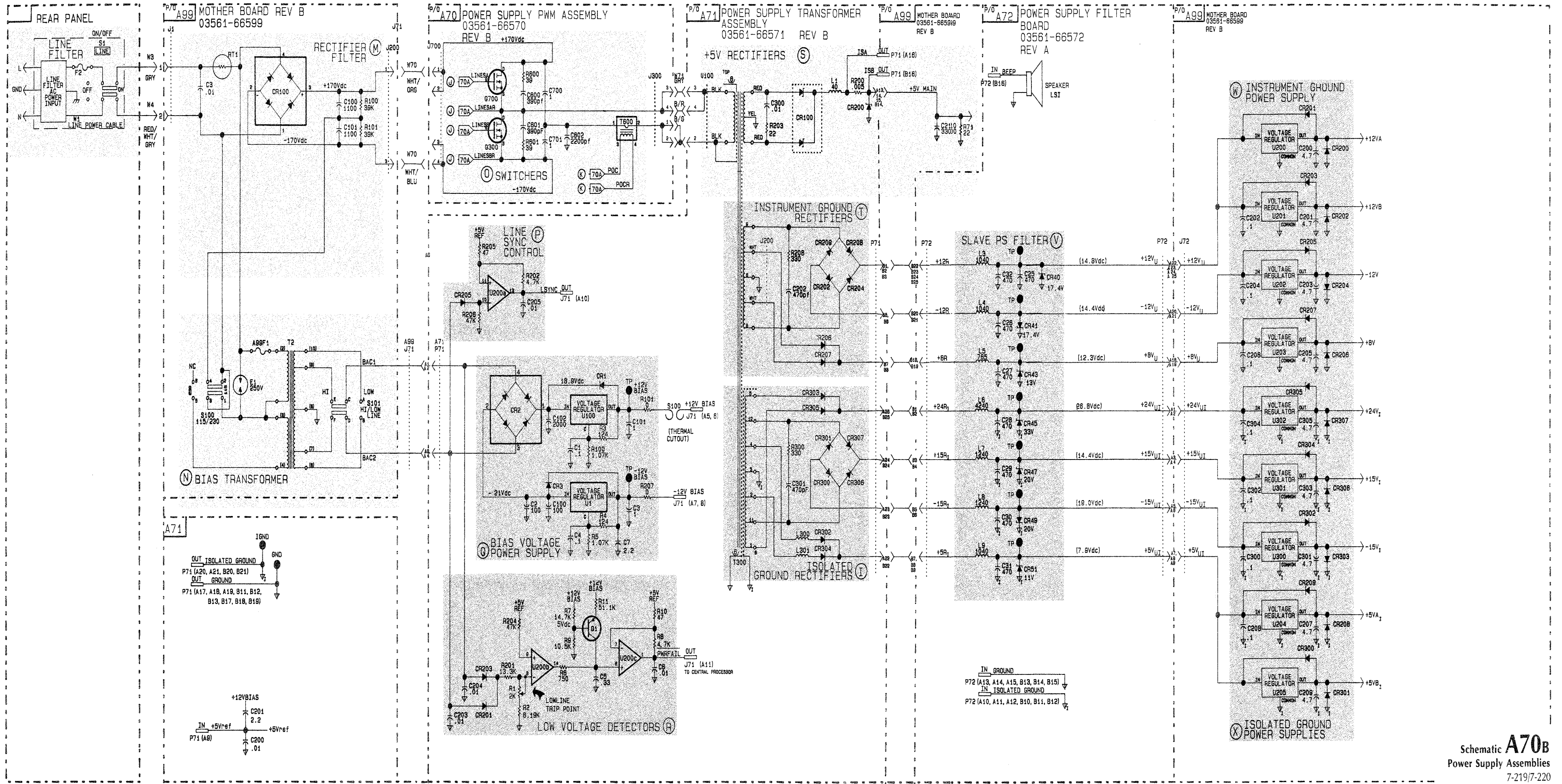
	+12VBIAS	-12VBIAS	+5V <sub>UI</sub>	-15V <sub>I</sub>	GND
U1	17				15
U2	7	4			
U3	7	4			
U101	8	1,4			8
U400	1				8
U401	7	4			
U402			3	12	
U500	16				8
U502	3				12





A71 Assembly

U200	+12VBIAS	GND
	3	12



## **7-31 A80 AND A81 KEYBOARD ASSEMBLIES**

### **7-32 Keyboard Driver Circuit Descriptions**

#### **GENERAL**

The front panel switches and LED's communicate with the processor over data lines PDB0 through PDB7. The processor can write to or read from the keyboard assembly. The processor periodically scans the keyboard to see if a switch has been pressed rather than working with an interrupt scheme. The individual blocks are explained in the text that follows.

#### **[A] ADDRESS I/O DECODING**

This circuitry is used to enable the various latches and drivers to accept or transmit data onto the front panel's internal bus. Processor address bits 0 and 1 are decoded by a 1 of 4 circuit. The four output lines are the enable lines for the functional blocks [C], [D] and [E].

#### **[B] PROCESSOR DATA BUS BUFFER**

This is a bi-directional 3-state device which interfaces the front panel with bits 0 through 7 of the data bus. The data direction and enable signals are  $PBR/\overline{W}$  (read/not write) and FPS (front panel scan).

#### **[C] SWITCH COLUMN DRIVE**

This circuitry contains an octal latch and eight inverting buffers. The 8-bit bus is applied to the column switch poles through these devices. When a switch is depressed, the column data is transferred to the row circuitry and read by the processor.

#### **[D] SWITCH ROW READ**

The switch row read is an octal receiver. When a switch is depressed, the column data is applied to the input. When the processor wants to read the key, it will enable the receiver to output via the switch row select. This output then goes through the processor data bus buffer to the processor's data bus.

#### **[E] LED DRIVE**

Two octal D-flops store the LED data sent from the processor board. This data is output through two resistor packs to the cathodes of the LED's. The LED's are not multiplexed but rather enabled continuously.



### 7-33 Removing The Front Panel

**WARNING**

*Disconnect the main power cord before attempting to remove the front panel.*

The following procedure outlines the steps necessary to remove the front panel.

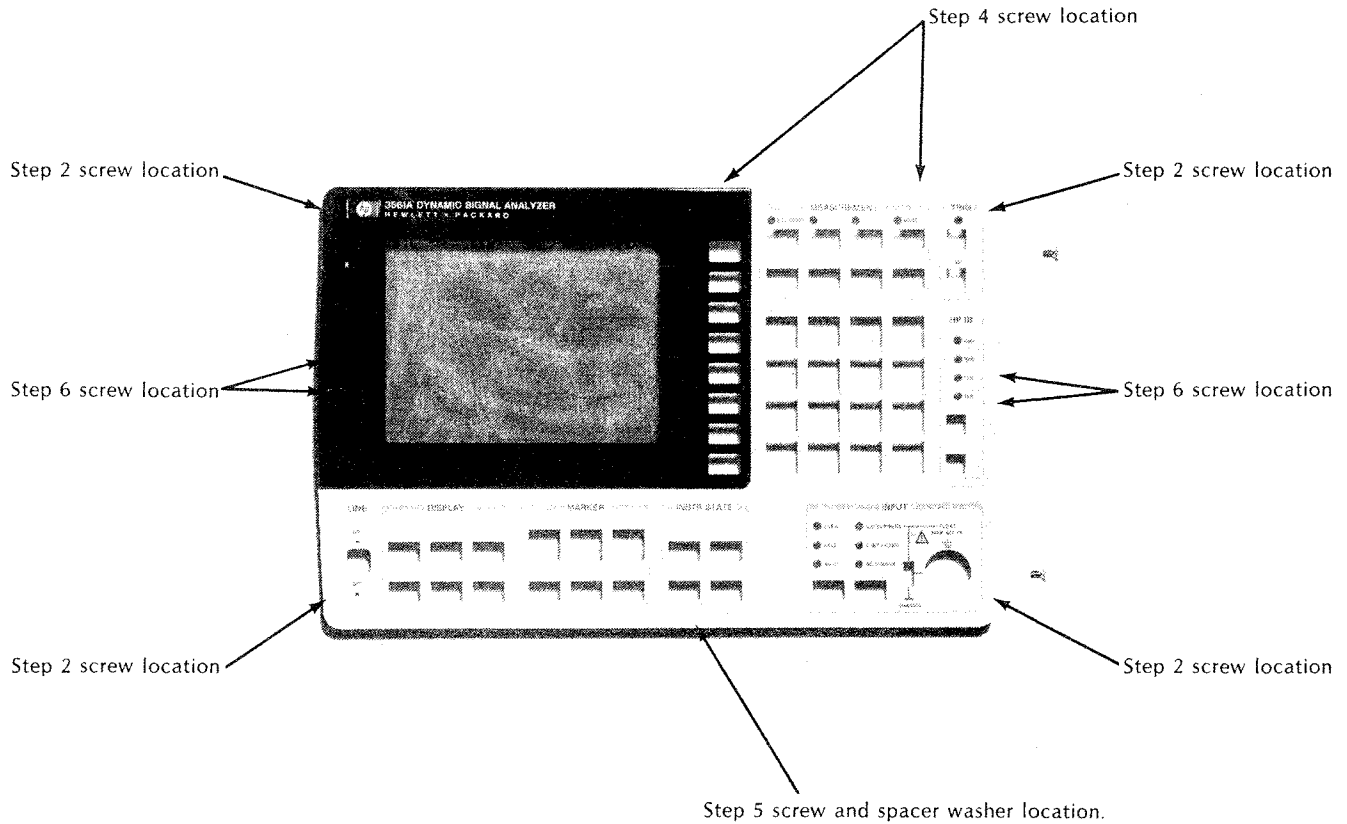
1. Remove the instrument's top and bottom covers.

**WARNING**

*+8000 Vdc is present at all times in the flyback transformer and CRT EVEN WITH THE MAIN POWER CORD REMOVED. Be extremely careful when working in proximity to this area. The high voltage could cause serious personal injury or death if contacted.*

2. Remove the four screws which secure the dress panel to the front panel casting. Refer to Figure 7-51 for their location.
3. Press the top dress panel tab on either side to remove the dress panel from the front panel casting.
4. Remove the two screws on the top right of the front panel casting which hold it to the aluminum board guide bracket. The location is shown in Figure 7-51. Do not remove the two screws over the CRT. These screws hold the CRT shield to the front panel.
5. Remove the screw and spacer washer from the bottom center of the front panel casting. The location is shown in Figure 7-51.
6. Remove the four screws holding the front panel casting to the left and right side rails as shown in Figure 7-51.
7. Remove the input cable W10 from the A10 Input Amplifier Assembly by pulling the A10 connector away from the A10 Assembly toward the front of the instrument.

**Figure 7-51 Front Panel Disassembly Screw Locations**



The front panel can now be pulled away from the instrument frame. If the black and white wire assembly going from the Motherboard Assembly to the CRT yoke is removed from the motherboard connector, the front panel can be placed flat in front of the instrument frame.

**WARNING**

*Do not damage or remove the green grounding wire which connects the front panel casting to the instrument's aluminum frame. Removing this wire will allow the front panel casting to float up to +8000 Vdc.*



*Be careful not to damage the ribbon cable W81 which connects the front panel circuitry with the instrument's motherboard assembly.*

## 7-34 Troubleshooting the A80 and A81 Keyboard Assemblies

### GENERAL

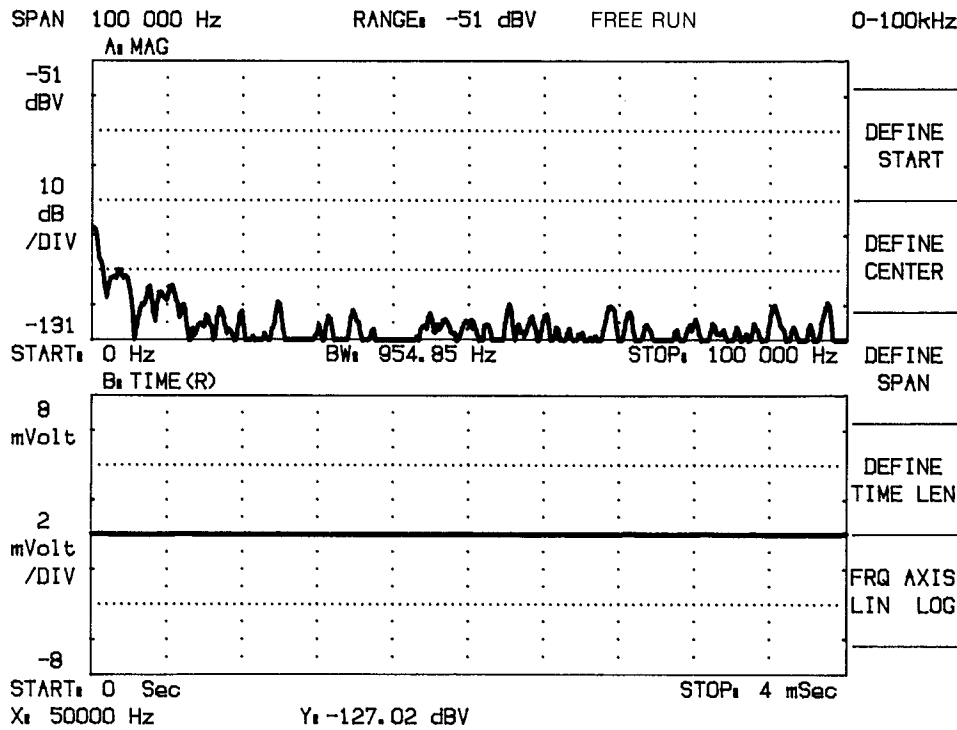
Failures on the A80 or A81 Keyboard Assemblies are not detected by the power-up test routine. There are also no built-in diagnostics which will test the keyboard assemblies and display an ERROR RETURN CODE should a failure exist. For these reasons, a list of keyboard failure symptoms is given in Table 7-58.

Signature analysis is used to troubleshoot the A81 Keyboard Driver Assembly.

**Table 7-58 Keyboard Failure Symptoms**

The following symptoms may occur if there is a failure on the keyboard assemblies:	
1.	During the power-up routine, the front panel LEDs should go through two lamp tests during which all LEDs should illuminate. If any of the LEDs do not illuminate, the failure may be on the A80 Keyboard Assembly. If none of the LEDs illuminate, the problem may be on the A81 Keyboard Driver Assembly.
2.	Immediately after the 10 second power-up routine, only the MEAS and AUTO LEDs should be illuminated. If either is not, the problem may be on the A80 Keyboard Assembly. If both are not, or there are any others illuminated, the problem may be on the A81 Keyboard Driver Assembly.
3.	Immediately after the 10 second power-up routine, the display shown in Figure 7-52 should appear on the CRT. Note particularly the definitions of the softkey menu. If the display does not match, there may be a stuck key on the A80 Keyboard Assembly. Check all keys and make sure that none are stuck in. There may also may be a shorted trace on the A80 Keyboard Assembly traces.
4.	Immediately after the 10 second power-up routine, if the CRT display continually flashes and the internal beeper continually sounds, there may be a stuck key or shorted trace on the A80 Keyboard Assembly.
5.	During instrument operation, pressing one of the front panel keys has no affect.
6.	During operation, pressing one of the front panel keys does not illuminate the correct LED indicator.
7.	Some or all of the HP-IB LED indicators does not illuminate during HP-IB operation and the instrument is operating properly under remote control.

**Figure 7-52 Correct Power-up CRT Display**



**A81 KEYBOARD TROUBLESHOOTING**

To troubleshoot the A80 and A81 Keyboard Assemblies, the front panel must be removed by following the instructions in Paragraph 7-33. However, to repair or replace either of the two assemblies, they must be removed from the front panel casting and separated.

With the front panel removed, the A81 Keyboard Driver Assembly is exposed. The A80 Keyboard Assembly is between the A81 Assembly and the front panel casting. The two assemblies make electrical contact through W80 which is a foam pressure cable. The foam supports one plane of fine wires. If these assemblies are pulled apart for repair, make certain that W80 is oriented properly with the fine wires making contact with the assembly connectors. Otherwise no contact will be made and the A80 Keyboard Assembly will not function.

To verify that the keyboard assemblies are causing symptoms 3 and 4, remove the keyboard interconnect cable W81 from the Motherboard Assembly and turn the instrument LINE switch ON.




**WARNING**

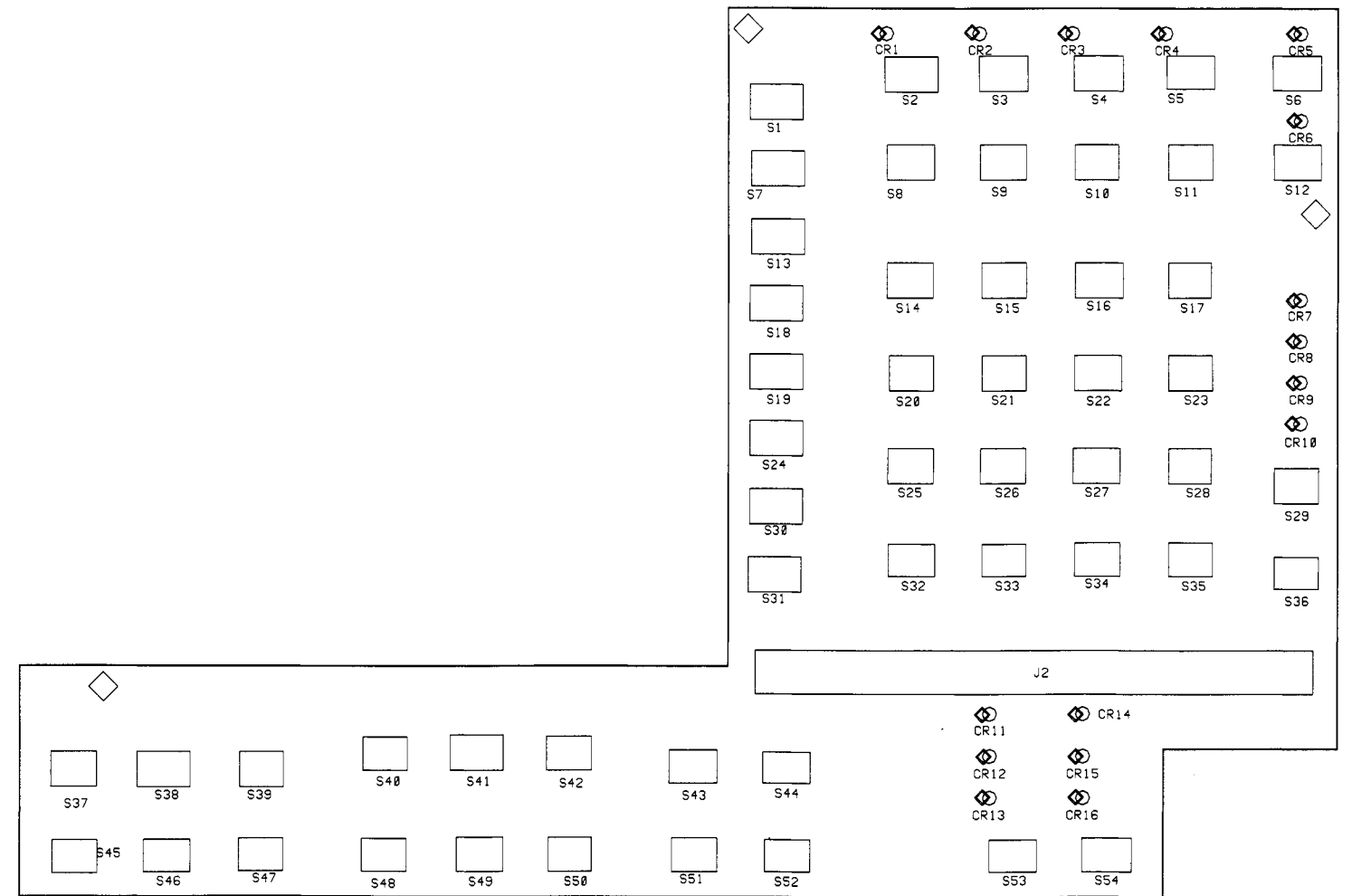
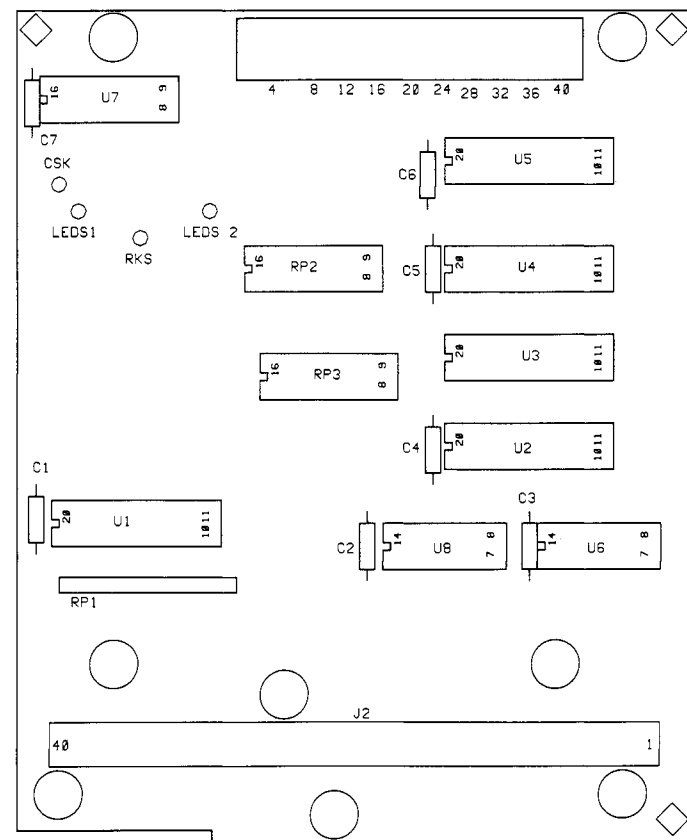
*The green grounding wire which connects the front panel casting to the mainframe sheet metal must be connected and making good contact. If this wire is missing or not making good contact, the front panel will float up to +8000 Vdc!*

If the instrument powers-up correctly, there is a problem with the Keyboard Assemblies. If however, the instrument still exhibits symptoms 3 and 4, there is a problem elsewhere in the instrument and you should refer to the fault isolation information in Section 6. Refer to Table 7-59 for the keyboard DSA troubleshooting information.

1. With the power turned OFF, remove the A60 Digital Display Driver Assembly (this disables the internal beeper which is activated during this test).
2. Move A40W1 from the left position to the right position as shown:
3. Turn the instrument ON and wait approximately 10 seconds before checking the signatures in Table 7-59.

**Table 7-59 Keyboard DSA Troubleshooting Information**

<b>Connect the Signature Analyzer as follows:</b>																																																																																																												
<b>Signal</b>	<b>Polarity</b>	<b>Connection</b>																																																																																																										
Clock		A81 TP FPS																																																																																																										
Start		A40 CR1 (Green LED Cathode)																																																																																																										
Stop		A40 CR1 (Green LED Cathode)																																																																																																										
+5 V Signature - 5UAH																																																																																																												
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U4(19)	U7F6																																																																																																											



**A81** KEYBOARD DRIVER ASSEMBLY

03561-66581  
REV A

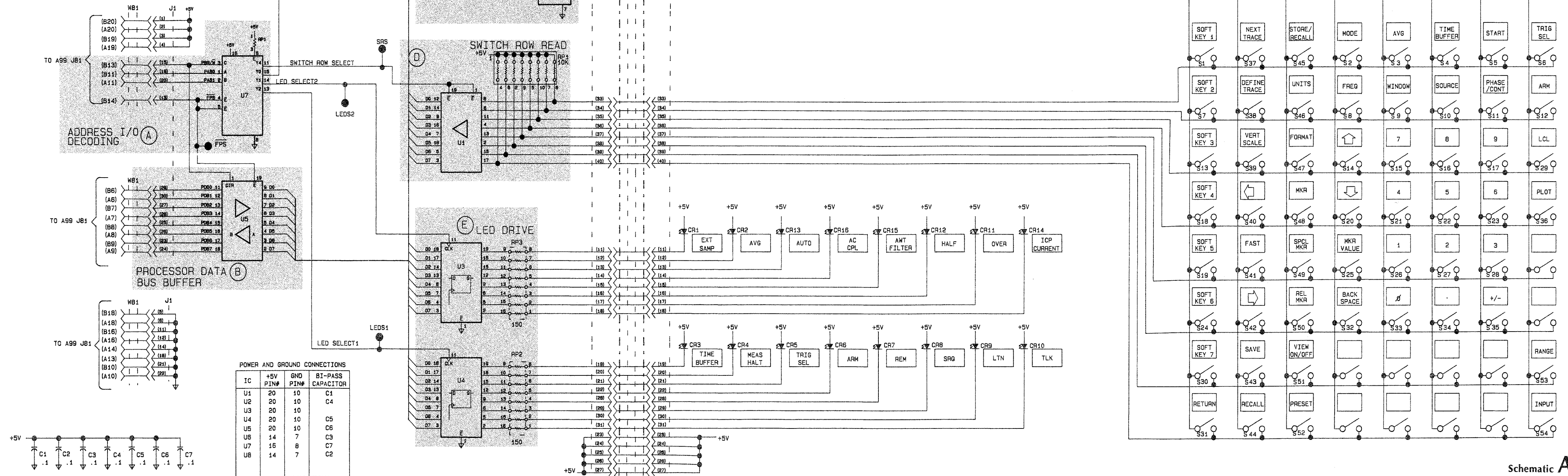
**A80** KEYBOARD

03561-66580  
REV A

INPUT			
SIGNAL NAME	FUNCTIONAL BLOCK	CONN# PIN#	ORIGIN
FPS	A	J1 (13)	A40
PAB0	A	J1 (19)	A40
PAB1	A	J1 (20)	A40
PBR/W	A	J1 (15)	A40
+5V		J1 (1, 2, 3, 4)	A70
GND		J1 (5, 6, 11, 12, 14, 15, 21, 22)	A70

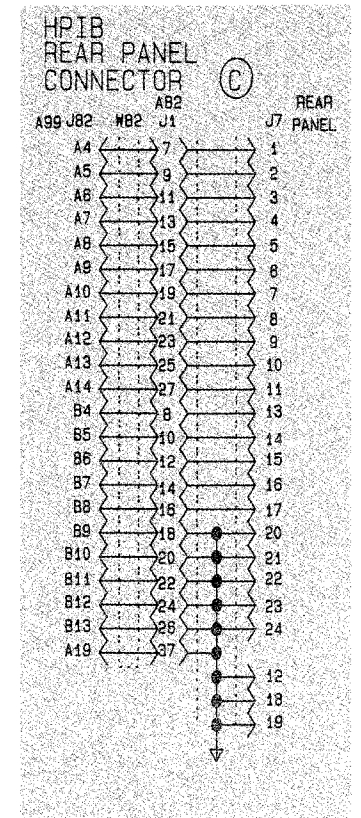
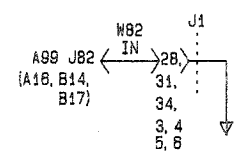
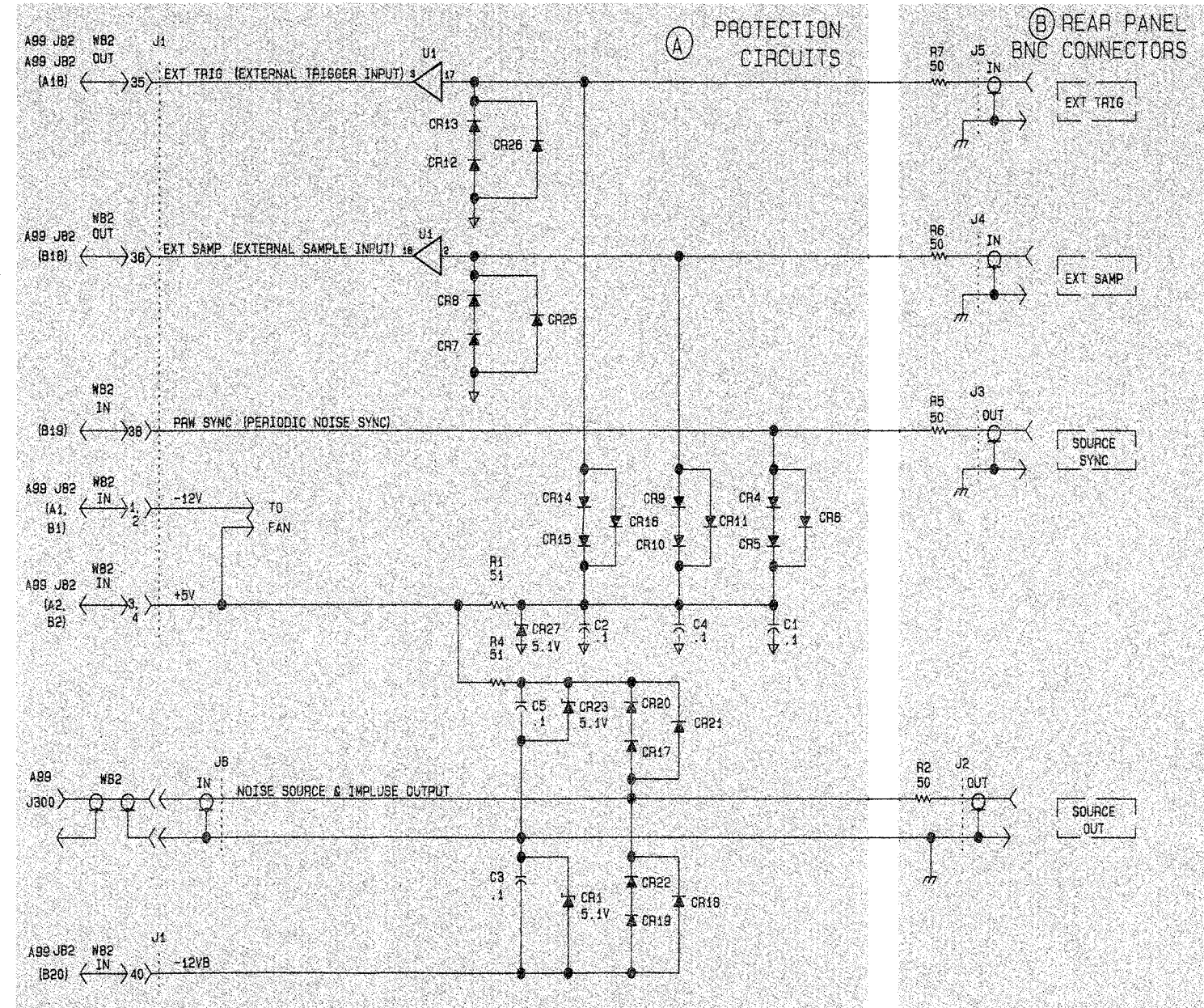
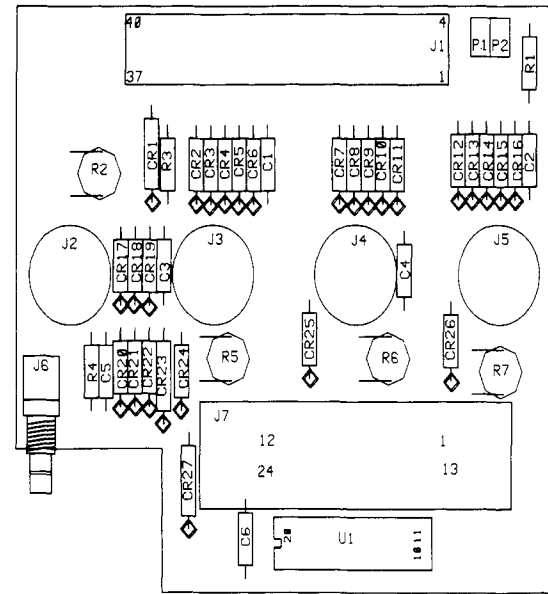
I/O			
SIGNAL NAME	FUNC. BLOCK	CONN# PIN#	ORIGIN
PDB0	B	J1 (29)	A40
PDB1	B	J1 (30)	A40
PDB2	B	J1 (27)	A40
PDB3	B	J1 (28)	A40
PDB4	B	J1 (25)	A40
PDB5	B	J1 (26)	A40
PDB6	B	J1 (23)	A40
PDB7	B	J1 (24)	A40

POWER AND GROUND CONNECTIONS			
IC	+5V PIN#	GND PIN#	BI-PASS CAPACITOR
U1	20	10	C1
U2	20	10	C4
U3	20	10	
U4	20	10	C5
U5	20	10	C6
U6	14	7	C3
U7	16	8	C7
U8	14	7	C2





**A82** REAR PANEL ASSEMBLY  
 03561-66582  
 REV B



## **7-36 A90 ANALOG DISPLAY DRIVER ASSEMBLY AND PART OF A99 MOTHERBOARD ASSEMBLY**

### **7-37 Analog Display Driver Circuit Description**

#### **GENERAL**

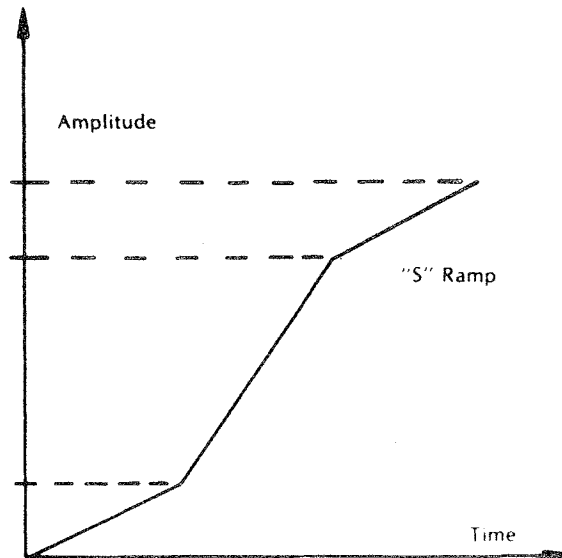
The main function of the analog display driver is to provide the CRT bias voltages and drive signals. The -hp-3561A uses a magnetic deflection CRT with a raster scan CRT sweep pattern. The raster scan pattern consists of a 512 horizontal by 256 vertical grid on the CRT screen. Each grid position is called a pixel. A pixel is illuminated when it is hit by the electron beam inside the CRT. This beam is turned on and off by the cathode drive signal and can be moved to any part of the CRT by a magnetic field created by the yoke. The yoke has two control inputs; vertical position control and horizontal position control. With the horizontal and vertical beam controls, the beam is swept down each vertical column of pixels, starting with the left most column and moving to the right. When all 512 columns of pixels have been covered, the beam is blanked and retraces to the start position. With this sweep pattern there are 512 vertical sweeps for each horizontal sweep, thus the vertical sweep is called the fast sweep and the horizontal sweep is called the slow sweep. The slow sweep operates at the power line frequency when jumper A60J200 is in the SYNC position and at 62.8 Hz when jumper A60J200 is in the 60 Hz position. The fast sweep operates at 36 kHz.

#### **[A] VIDEO DRIVE**

The video drive circuit provides the cathode drive signal (CATHD) which turns the CRT beam on or off. When the VIDH and the VIDF signals are both high, the CATHD signal is pulled high to +14.8 Vdc through Q203. This turns the CRT beam off. When the VIDF (video full bright) signal goes low, the CATHD signal is pulled low to -12 Vdc through Q202. This turns CRT beam on full intensity. When the VIDH (video half bright) goes low, the CATHD signal is pulled low to  $-9 \text{ Vdc} \pm 3 \text{ Vdc}$ , (depending on the position of the half bright adjustment), through Q205. This turns the CRT beam on half intensity. The +12V<sub>U</sub> volt supply is an unregulated supply and may vary in voltage around +14.8 Vdc.

#### **[B] SLOW SWEEP HORIZONTAL DRIVE**

The slow sweep circuit generates an "S" shaped ramp signal used to drive the horizontal position of the yoke. This ramp is generated from the SSYNC signal which is output from the A60 Assembly. When SSYNC is high, Q400 is turned off allowing the current source (Q3) to charge C400 creating a ramp at TP100. When SSYNC goes low, Q400 is turned on pulling the voltage across C400 to ground. Feedback around C400 is provided to put an "S" shape into the ramp. This feedback loop uses CR1 and CR2 to divide the ramp into three sections. The "S" shape is created by giving the center section a larger gain as shown in Figure 7-53.

**Figure 7-53 "S" Ramp****[D] FAST SWEEP VERTICAL DRIVE, [E] FLYBACK TRANSFORMER**

The fast sweep circuit works in conjunction with the flyback transformer to generate a ramp signal to drive the vertical control of the yoke. The FSYNC (fast sync) signal generated on the A60 Assembly establishes the frequency of the vertical ramp. At power-on, capacitors C9, C102, and C103 all charge up to approximately +30 Vdc. These capacitors then provide constant voltages to power the flyback transformer. When PDRIVE goes high, Q1 on the A99 Assembly is turned on, shorting pin three of the flyback transformer to ground. This causes C102 to discharge through the vertical yoke coil, creating a ramp. When PDRIVE goes low, Q1 on the A99 Assembly is turned off causing a large current surge from the flyback transformer. The current surge charges C102 through the vertical yoke coil causing the CRT beam to retrace. Feedback of the retrace pulse is provided through the PSENSE signal. This feedback works to align the rising edge of PSENSE with the falling edge of FSYNC by changing the ON time of the PDRIVE signal. If the edges of the FSYNC and PDRIVE signals are not aligned, the display pattern will not be vertically centered on the CRT screen.

The matching between the flyback transformer, T100, and capacitors A99 C5, C6, C7, and C8 determines the retrace pulse width and the value of the CRT anode voltage. Whenever T100 is replaced, these capacitors must be re-selected using the procedures given in Section 7-38.

**[F] HIGH VOLTAGE**

The high voltage circuit uses two taps from the flyback transformer to generate the grid bias voltages for the CRT. When the PDRIVE signal goes low, a current surge is generated in the flyback transformer which causes a +450 Volt peak and a -150 Volt peak voltage spike. These voltages are low pass filtered and divided down to drive the CRT grids.

**Table 7-60 A90 Assembly Signal Descriptions**

<b>Signal</b>	<b>Description</b>
CATHD	CATHode Drive: Turns the CRT beam on or off; the voltage of this signal relative to the voltage of the BRIGHTNESS signal determines the intensity of the CRT beam.
FDRIVE	Fast Sweep Yoke DRIVE: Powers the vertical yoke coil.
FDRIVER	Fast Sweep Yoke DRIVE Return: Current return from the vertical yoke coil.
FSYNC	Fast Sweep SYNChronizer: This signal synchronizes the fast sweep trace with the slow sweep trace and the cathode drive signal.
PDRIVE	Pulse Drive: Initiates a retrace pulse on falling edge of PDRIVE.
PSENSE	Pulse SENSE: Detects a retrace pulse. Provides feedback to vertically center the display on the CRT screen.
RTRC	ReTRaCe: This signal is the PSENSE signal clipped to +5 Volts and indicates when a retrace is occurring.
SDRIVE	Slow Sweep Yoke DRIVE: Powers the horizontal yoke coil.
SDRIVER	Slow Sweep Yoke DRIVE Return: Current return from the horizontal yoke coil.
SSHAPE	S SHAPE: Provides feedback to put an "S" shape into the slow sweep ramp.
SSYNC	Slow Sweep SYNChronizer: This signal synchronizes the slow sweep trace with the fast sweep trace and the cathode drive signal.
VIDH	VIDeo Drive Half Bright: Turns the CRT beam on half intensity.
VIDF	VIDeo Drive Full Bright: Turns the CRT beam on full intensity.

## 7-38 Troubleshooting the Analog Display Driver

### SAFETY CONSIDERATIONS

Troubleshooting the analog display driver may require placing the A90 Assembly on an extender board or removing the plastic shield from the bottom of the A99 Motherboard Assembly exposing dangerous voltages. Service should only be performed by service trained personnel who are aware of the hazards involved. Hazardous voltage areas are outlined in red on the schematic diagram and component locators. Use extreme care when troubleshooting in these areas.

#### WARNING

*8000 Vdc are present at all times in the flyback transformer and CRT EVEN WHEN THE INSTRUMENT IS TURNED OFF. Be extremely careful when working in proximity to this area. The high voltage can cause serious personal injury if contacted.*

#### WARNING

*Power Supply Capacitors on the A99 Motherboard Assembly will remain charged to  $\pm 170$  Vdc for at least three (3) minutes after power is removed from the instrument. These voltages are exposed when the protective plastic shield is removed. Be extremely careful when working in proximity to this area. The high voltage can cause serious personal injury if contacted.*

#### WARNING

*+450 and -150 Volts are present on the A90 Analog Display Driver Assembly and the A99 Motherboard Assembly. Be extremely careful when working in proximity to this area. The high voltage can cause serious personal injury if contacted.*

### TROUBLESHOOTING AND REPLACING PARTS ON THE A99 MOTHERBOARD ASSEMBLY

All parts on the A99 Assembly should be checked by removing the protective plastic shield covering the bottom of the A99 Motherboard Assembly. The front panel should not be removed while power is applied to the instrument. Once a faulty component is isolated, the front panel can then be removed and the component replaced. Instructions for removing the front panel are given in Section 7-35 "A80 AND A81 KEYBOARD ASSEMBLIES"

**WARNING**

*Disconnect the power cord before removing the front panel and replace the front panel before re-applying power. Do not disconnect the green grounding wire connecting the front panel to the chassis. If this grounding wire is disconnected the front panel can charge up to 8000 Vdc.*

**General Troubleshooting**

By observing the characteristics of a display failure, the problem can usually be isolated to either the A90 Analog Display Driver Assembly or the A60 Digital Display Driver Assembly. If the CRT screen is completely blank, the failure could be related to any -hp-3561A assembly. Start the fault isolation procedure at TEST A to isolate these types of failures. The following display symptoms most likely indicate a failure in the A90 or A99 Analog Display Driver Assemblies:

- Vertical Position Incorrect
- Vertical Size Incorrect
- Horizontal Position Incorrect
- Horizontal Size Incorrect
- Brightness Will Not Adjust Correctly
- Focus Will Not Adjust Correctly
- Excessive Background Light

The following display symptoms most likely indicate a failure in the A60 Digital Display Driver Assembly, however, these symptoms can also be caused by the main processor. For information on isolating a failure to either the digital display driver or the main processor, see the fault isolation section of this manual.

- Random Dots Appear on the Screen
- Random Dots Missing on the Screen
- Failure Appearing Only on the Alpha Numerics
- Failure Appearing Only on the Graphics
- Graticule has Missing Lines, Missing Dots, or Extra Dots

The following display symptoms most likely indicate a failure in the CRT or yoke.

- Display Pattern Trapezoidal
- Display Pattern Tilted to one side or the other

The display adjustment procedures given in Section 2 of this manual should always be performed both before and after troubleshooting the A90 or A99 Assemblies.

**A60 ASSEMBLY TEST SETUP**

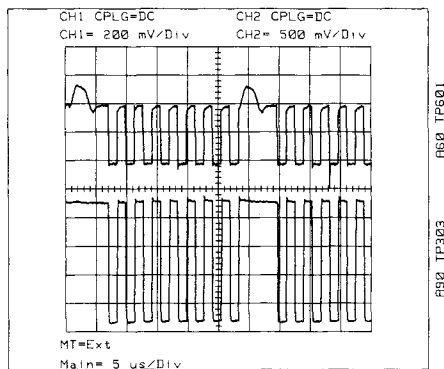
The A60 Assembly must be setup as shown below before troubleshooting the A90 and A99 Assemblies.

1. Turn the -hp-3561A LINE power switch OFF.
2. Move test jumper A60J100 to the PLANE2 position and jumper A60J200 to the 60 Hz position as shown on the A60 Assembly Component Locator.

**[A] VIDEO DRIVE**

With Jumper A60J100 in the PLANE2 test position, turn the -hp-3561A LINE power switch ON and check the waveforms given in Figure 7-54. Move test Jumper A60J100 to the PLANE1 test position and check the waveforms given in Figure 7-55.

**Figure 7-54 PLANE2 Video Drive Waveforms**



Probe: 10:1

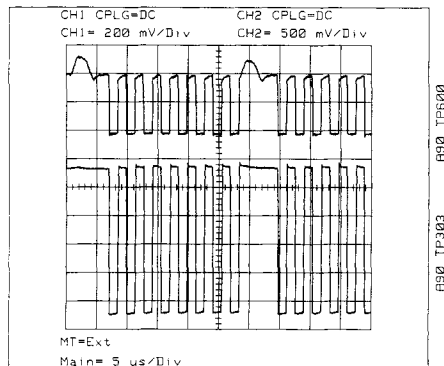
Ch1: Connection- A90 TP601 "VIDH"  
Coupling- dc  
Ground- Fourth Graticule From Top

Ch2: Connection- A90 TP303 "CATHD"  
Coupling- dc  
Ground- Second Graticule From Bottom

Trigger: External- A90 TP501 "SSYNC"  
Slope- Positive

Bandwidth Limit: OFF

**Figure 7-55 PLANE1 Video Drive Waveforms**



Probe: 10:1

Ch1- Connection- A90 TP600 "VIDF"  
Coupling- dc  
Ground- Third Graticule From Top

Ch2: Connection- A90 TP303 "CATHD"  
Coupling- dc  
Ground- Third Graticule From Bottom

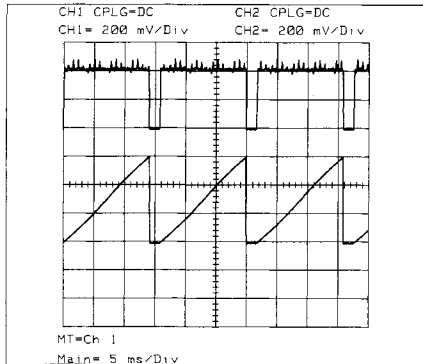
Trigger: External- A90 TP501 "SSYNC"  
Slope- Positive

Bandwidth Limit: OFF

**[B] SLOW SWEEP HORIZONTAL DRIVE**

Check the waveforms given in Figure 7-56 in the order given. Due to feedback, a failure in the voltage to current driver may cause an incorrect signal at the test point TP102.

**Figure 7-56 Slow Sweep Horizontal Drive Waveforms**



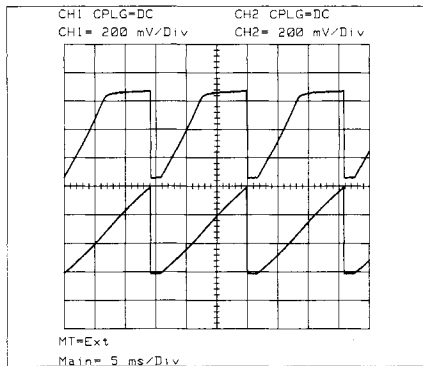
Probe: 10:1

Ch1: Connection- A90 TP501 "SSYNC"  
Coupling- dc  
Ground- Third Graticule from Top

Ch2: Connection- A90 TP100 "S Ramp"  
Coupling- dc  
Ground- Third Graticule from Bottom

Trigger: Internal- Ch1  
Slope- Positive

Bandwidth Limit: ON



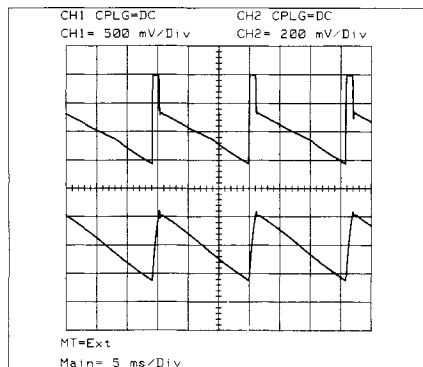
Probe: 10:1

Ch1: Connection- A90 TP1 "S Feedback"  
Coupling- dc  
Ground- Third Graticule from Top

Ch2: Connection- A90 TP100 "S Ramp"  
Coupling- dc  
Ground- Second Graticule from Bottom

Trigger: External- A90 TP501 "SSYNC"  
Slope- Positive

Bandwidth Limit: ON



Probe: 10:1

Ch1: Connection- A90 TP102  
Coupling- dc  
Ground- Third Graticule from Top

Ch2: Connection- A90 TP103 "SYDRIVER"  
Coupling- dc  
Ground- Third Graticule from Bottom

Trigger: External- A90 TP501 "SSYNC"  
Slope- Positive

Bandwidth Limit: ON

Note: The amplitude and dc offset of these signals will vary with the horizontal gain adjustment and the horizontal position adjustment.



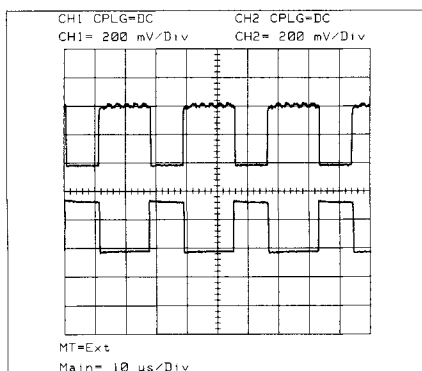
**[D] FAST SWEEP VERTICAL DRIVE, [E] FLYBACK TRANSFORMER**

The fast sweep vertical drive circuit should be tested first in open loop mode and then in closed loop mode. To break the PSENSE feedback loop, use a clip lead to short the two pins of A90J400 together. With A90J400 shorted, check the waveforms given in Figure 7-57 in the order given. If all of the waveforms in Figure 7-57 are correct, close the feedback loop by removing the clip lead shorting A90J400 and check the waveforms given in Figure 7-58.

**NOTE**

*When A90 J400 is shorted, the display will appear to be vertically off center and will appear to wrap around the end of the screen.*

**Figure 7-57 Fast Sweep Waveforms in Open Loop Mode**



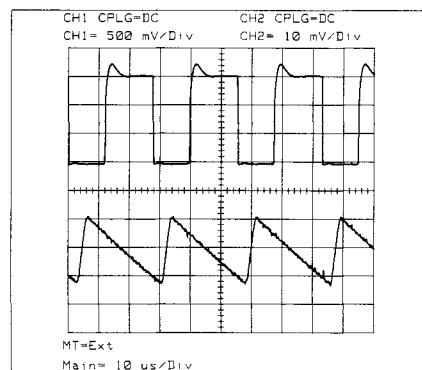
Probe: 10:1

Ch1: Connection- A90 TP507 "FSYNC"  
Coupling- dc  
Ground- Fourth Graticule from Top

Ch2: Connection- A90 TP505 "LOW PDRIVE"  
Coupling- dc  
Ground- Third Graticule from Bottom

Trigger: External- A90 TP501 "SSYNC"  
Slope- Positive

Bandwidth Limit: ON



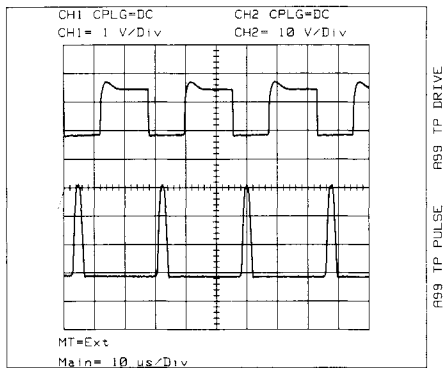
Probe: 10:1

Ch1: Connection- A90 TP506 "PDRIVE"  
Coupling- dc  
Ground- Fourth Graticule from Top

Ch2: Connection- A99 TP "RAMP"  
Coupling- dc  
Ground- Third Graticule from Bottom

Trigger: External- A90 TP501 "SSYNC"  
Slope: Positive

Bandwidth Limit: ON



Probe: Ch1- 10:1 Probe on Ch1  
 Ch2- 10:1, 10 MΩ, Maximum Voltage  
 ≥ 600 Vdc  
 (-hp-10014A)

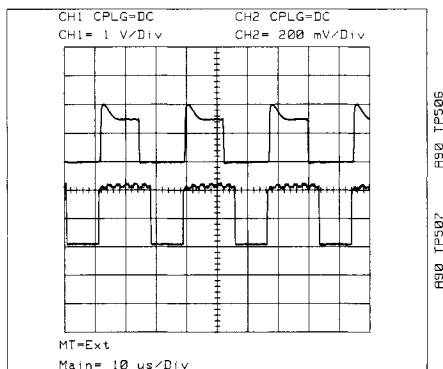
Ch1: Connection- A99 TP“DRIVE”  
 Coupling- dc  
 Ground- Third Graticule from Top

Ch2: Connection- A99 TP“PULSE”  
 Coupling- dc  
 Ground- Second Graticule from Bottom

Trigger: External- A90 TP501 “SSYNC”  
 Slope- Positive

Bandwidth Limit: ON

Figure 7-58 Fast Sweep Waveforms in Closed Loop Mode



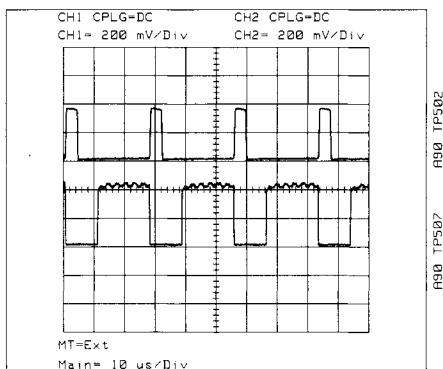
Probe: 10:1

Ch1: Connection- A90 TP506 “PDRIVE”  
 Coupling- dc  
 Ground- Fourth Graticule from Top

Ch2: Connection- A90 TP507 “FSYNC”  
 Coupling- dc  
 Ground- Third Graticule from Bottom

Trigger: External- A90 TP501 “SSYNC”  
 Slope- Positive

Bandwidth Limit: ON



Probe: 10:1 Probe on Ch1 and Ch2

Ch1: Connection- A90 TP502 “LOW PSENSE”  
 Coupling- dc  
 Ground- Fourth Graticule from Top

Ch2: Connection- A90 TP507 “FSYNC”  
 Coupling: Dc  
 Ground- Third Graticule from Bottom

Trigger: External- A90 TP501 “SSYNC”  
 Slope- Positive

**[F] HIGH VOLTAGE, [C] CATHODE RAY TUBE****WARNING**

*8000 Vdc present at all times in the flyback transformer and CRT EVEN WHEN THE INSTRUMENT IS TURNED OFF. Be extremely careful when working in proximity to this area. The high voltage could cause serious personal injury if contacted.*

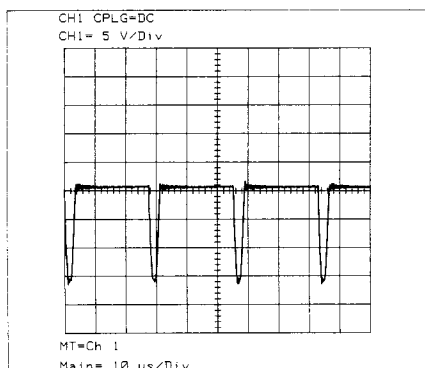
*Use only high voltage probes with the specified characteristics when troubleshooting the high voltage circuits.*

Before checking the high voltage signals, check for proper operation of the CRT heater. If the heater is operating correctly, there will be an orange glow at the back of the CRT.

A 10 M $\Omega$  10:1 probe (-hp-10014A) which meets the required characteristics listed in Table 1-5 is required to check the +450 V<sub>peak</sub> and the -150 V<sub>peak</sub> waveforms of the flyback transformer. Lower impedance probes will load the high voltage circuit down, changing its operating characteristics. Check the high voltage waveforms given in Figure 7-59.

A 1000 M $\Omega$ , 1000:1 high voltage probe (-hp-34111A) which meets the required characteristics listed in Table 1-5 is required to check the 8000 Vdc CRT anode voltage. To measure this voltage, touch the tip of the probe to the anode cap as shown in Figure 7-60. The voltage should be 8200 Vdc  $\pm$  820 Vdc.

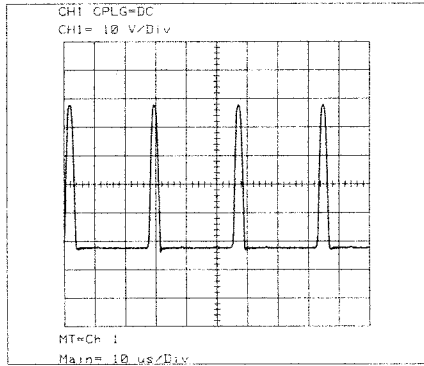
**Figure 7-59 High Voltage Waveforms**



Probe: 10:1, 10 M $\Omega$ , Maximum Voltage  
 $\geq$  600 Vdc  
(-hp-10014A)

Ch1: Connection- A90 TP900 "-150 V<sub>peak</sub>"  
Coupling- dc  
Ground- Center Graticule

Trigger: Internal- Ch1  
Slope- Negative

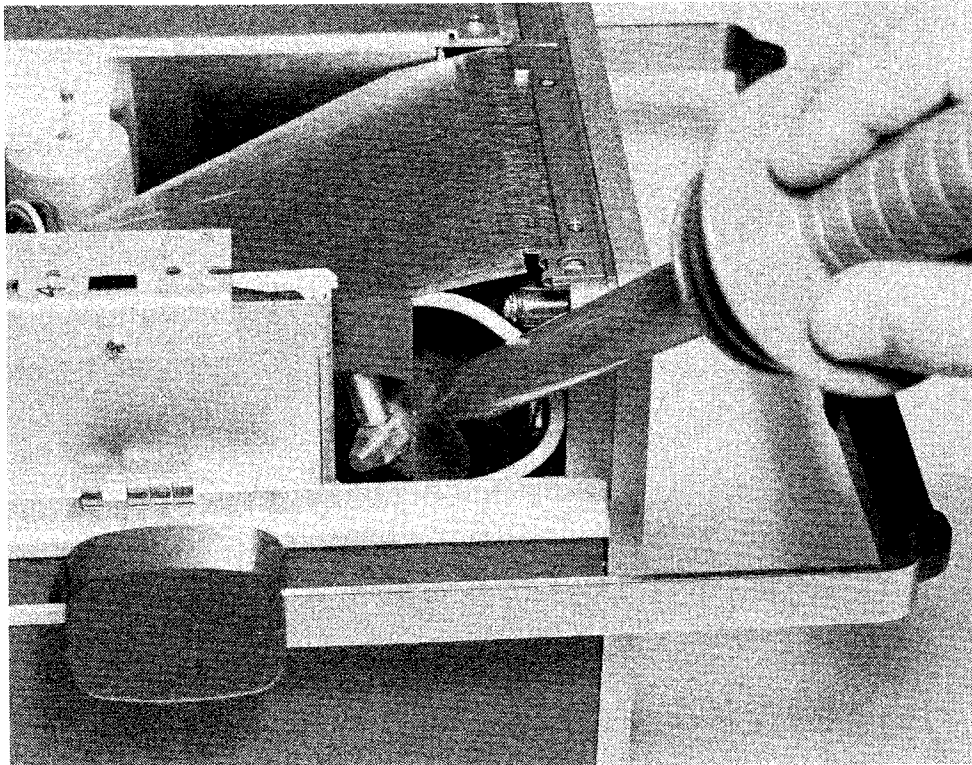


Probe: 10:1, 10 MΩ, Maximum Voltage  
 ≥ 600 Vdc  
 (-hp-10014A)

Ch1: Connection- A90 TP304 “+450 Vpeak”  
 Coupling- dc  
 Ground- Third Graticule from Bottom

Trigger: Internal- Ch1  
 Slope- Positive

Figure 7-60 Measuring the CRT Anode Voltage



SELECTING A99 C5, C6, C7, AND C8

**WARNING**

*Review the “Safety Considerations” and “Troubleshooting and Replacing Parts on the A99 Motherboard Assembly” paragraphs in this section before performing these procedures.*

The matching between the flyback transformer, T100, and capacitors A99 C5, C6, C7, C8 determines the retrace pulse width and the CRT anode voltage. Whenever T100 is replaced, these capacitors must be reselected using the procedures given below. Capacitors C5, C6, C7, and C8 can each be loaded with any of the capacitor values given in Table 7-61, with the optimum loaded values given in Table 7-62. The optimum values will be correct for most transformers and is the usual factory loaded configuration.

**Table 7-61 Possible Values for A99 C5, C6, C7, C8**

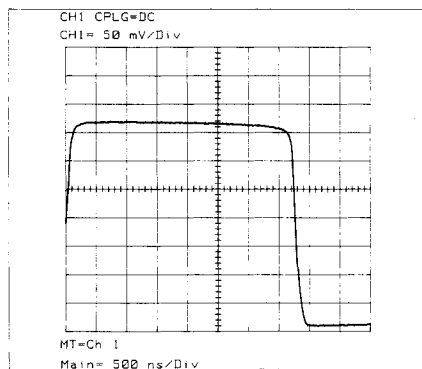
Capacitor Value	Maximum Voltage	-hp-Part Number
not loaded		
220 pF	1000 Vdc	0160-3454
470 pF	1000 Vdc	0160-3455
1000 pF	1000 Vdc	0160-3466

**Table 7-62 Optimum Loaded Values for A99 C5, C6, C7, C8**

Capacitor	Optimum Value
C5	1000 pF
C6	1000 pF
C7	not loaded
C8	not loaded

1. Connect the oscilloscope probe to A90TP502, turn the -hp-3561A LINE power switch ON, and set the oscilloscope to obtain the waveform given in Figure 7-61. Set the oscilloscope ground to the bottom graticule.

**Figure 7-61 Retrace Pulse Width Measurement**



Probe: 10:1

Ch1: Connection- A90 TP502 "RTRC"  
Coupling- dc  
Ground- Bottom Graticule

Trigger: Internal- Ch1  
Slope- Positive

2. Measure the width of the "RTRC" pulse at the center horizontal graticule. The pulse width should be 3.7 microseconds  $\pm$  .15 microseconds ( $\pm$  1.5 minor division).
3. If the pulse width is too narrow, increase the total capacitance of C5 + C6 + C7 + C8 by adding 230 pF for every .1 microseconds that the pulse width is too narrow. (e.g., If the pulse width is 3.5 microseconds wide, add a 470 pF capacitor to any one of the unloaded positions to bring the pulse width up to 3.7 microseconds.)

If the pulse width is too wide, decrease the total capacitance of C5 + C6 + C7 + C8 by deleting 230 pF for every .1 microseconds that the pulse width is too wide. (eg., If the pulse width is 3.9 microseconds wide, replace one of the 1000 pF capacitors with a 470 pF capacitor to bring the pulse width down to 3.7 microseconds.

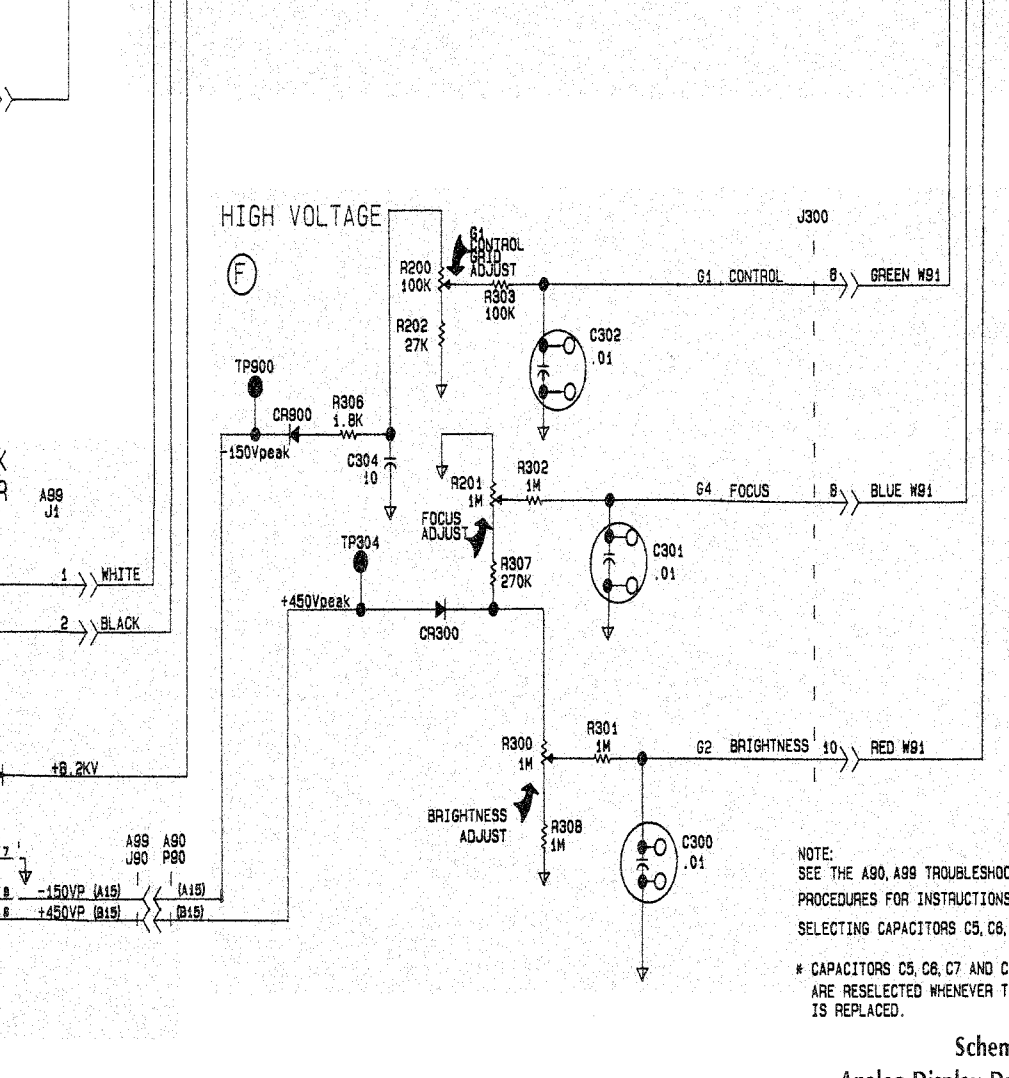
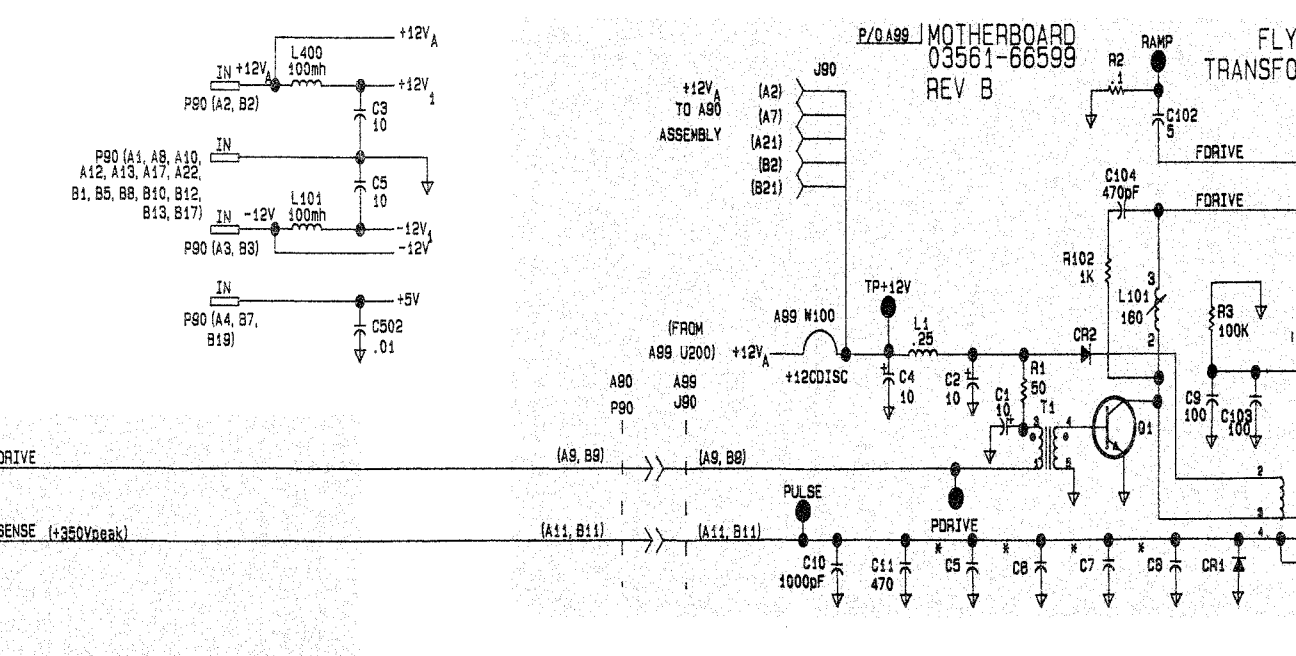
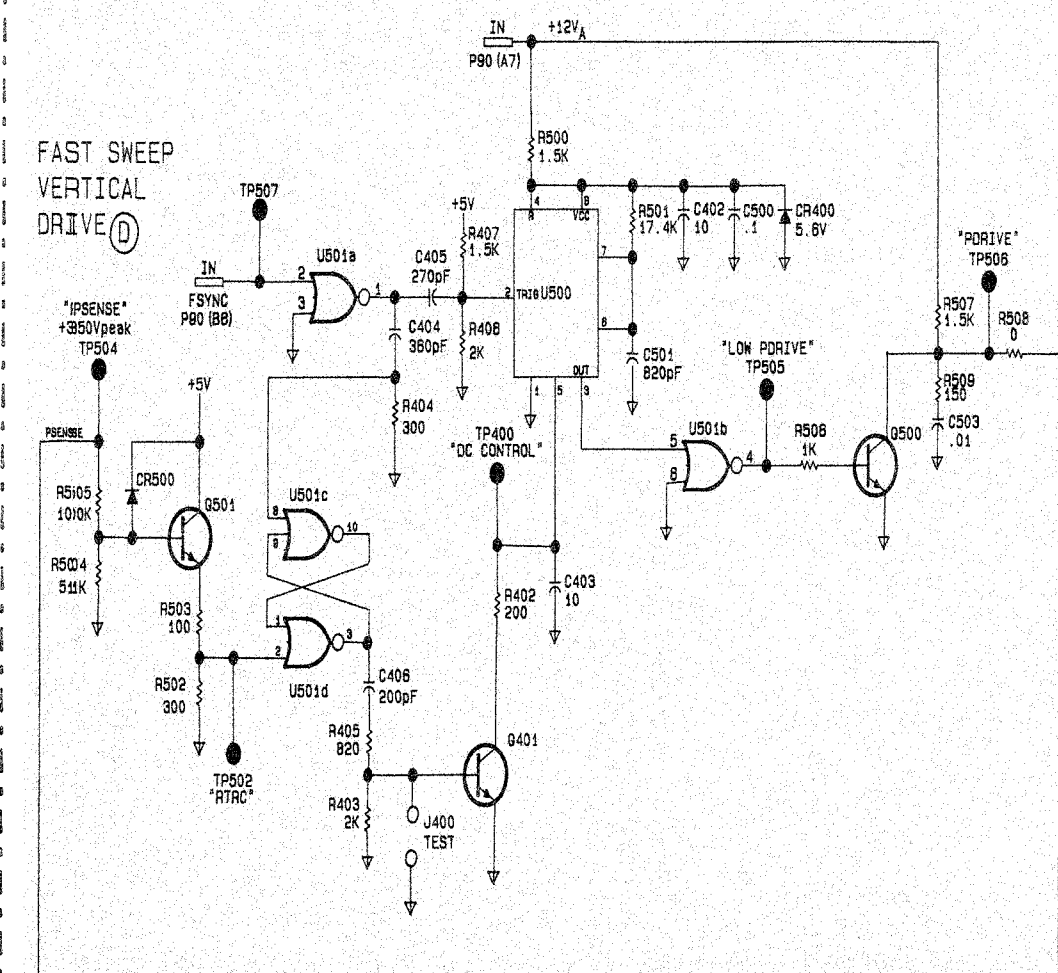
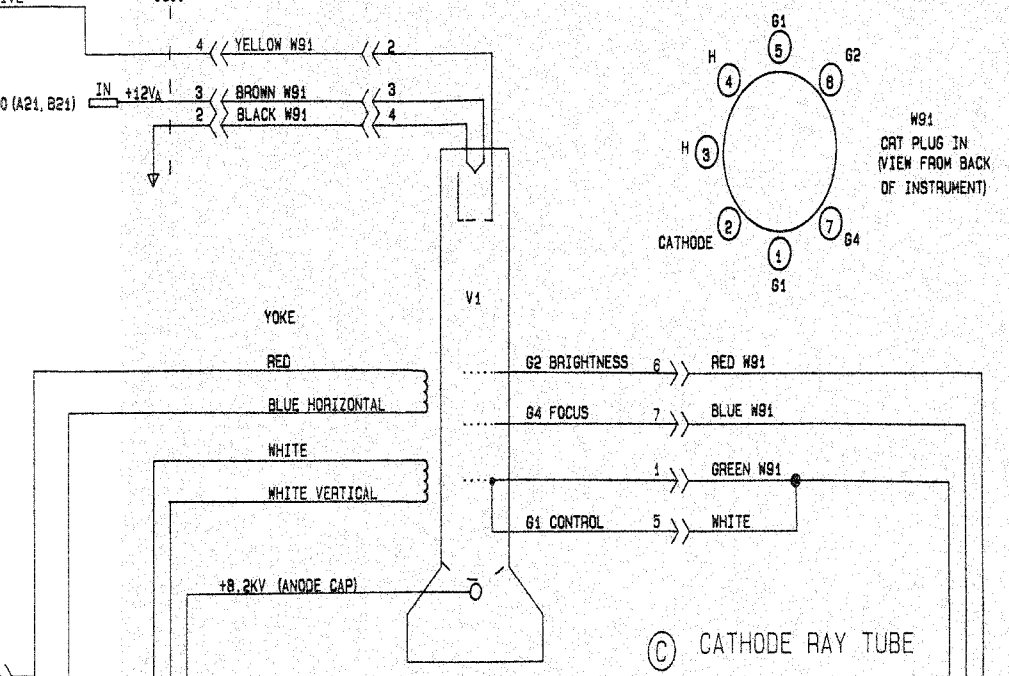
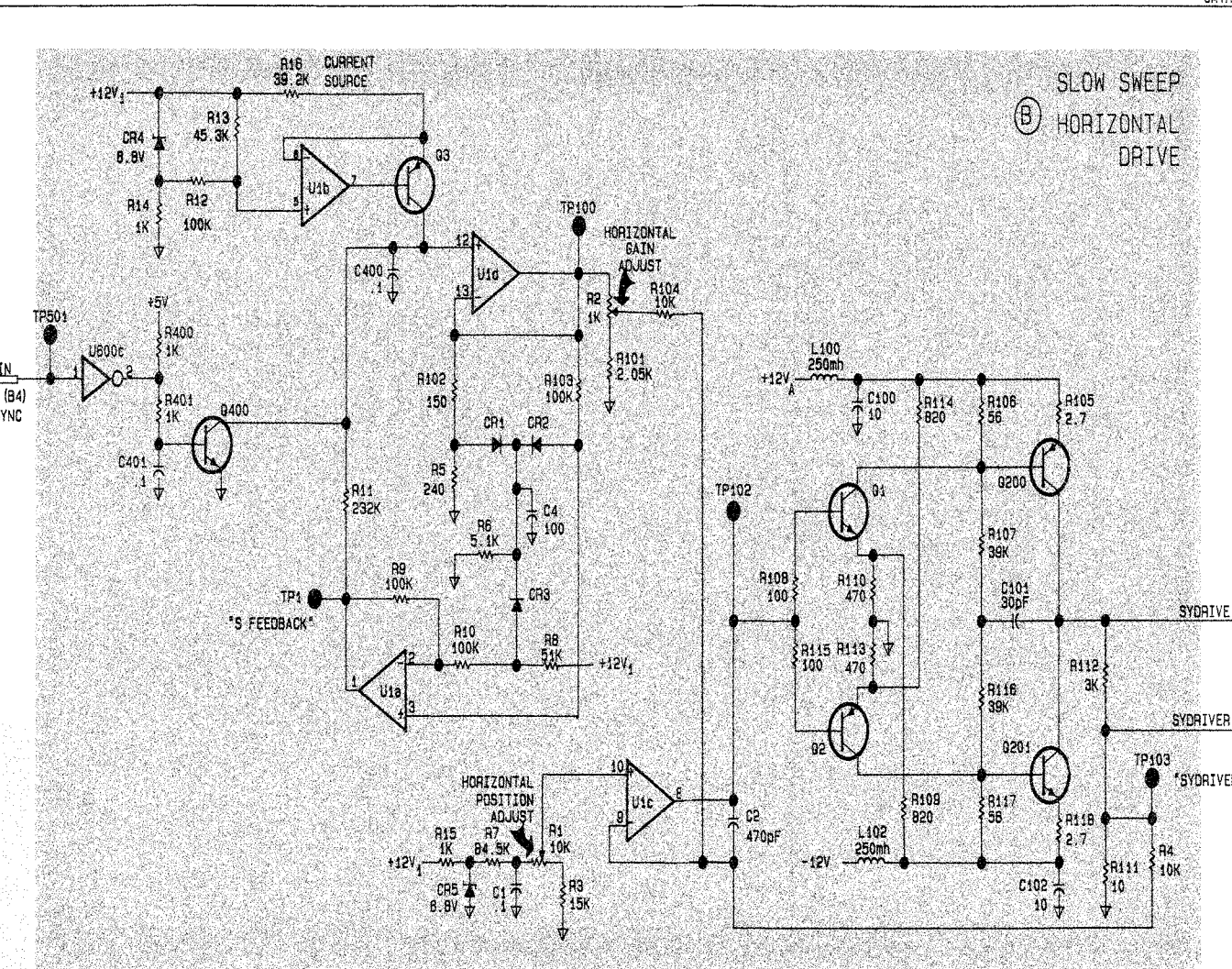
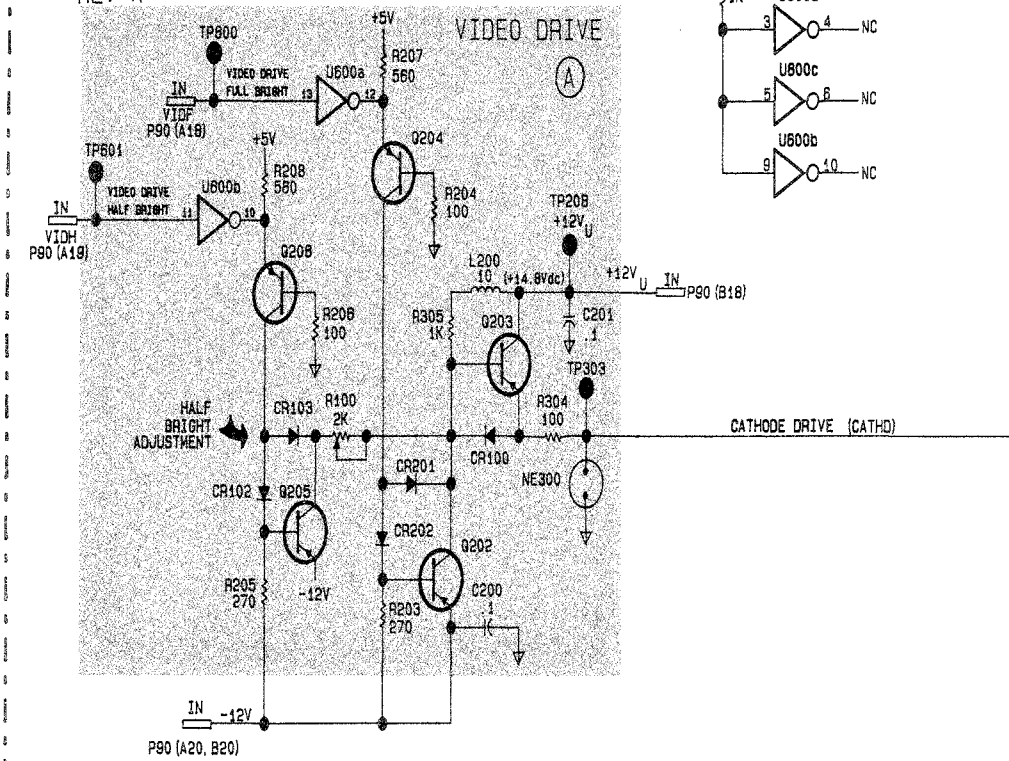
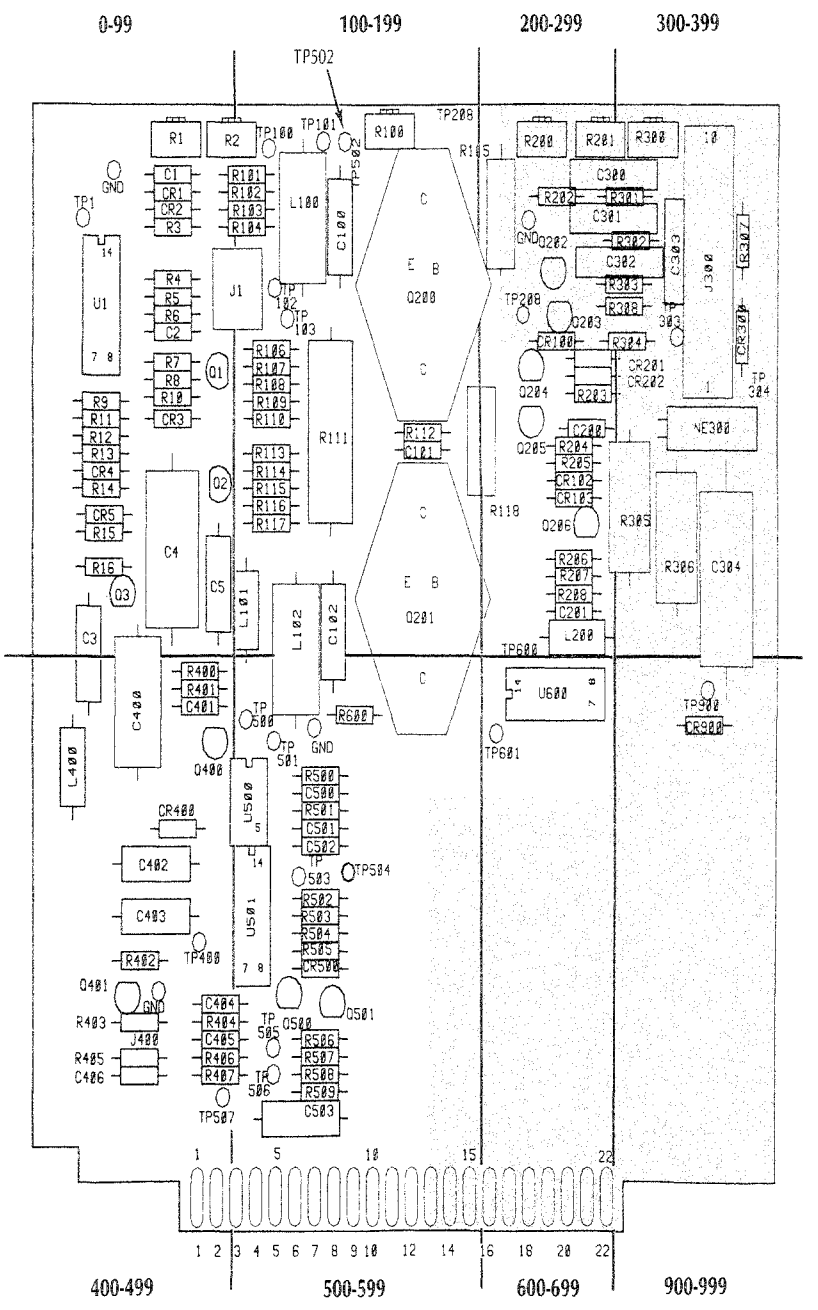
**Table 7-63 A90 Assembly Signal Connections**  
**INPUTS**

Signal Name	Functional Block	Connector Number	Origin Assemblies
FSYNC	D	P90(B6)	A60
SSYNC	B	P90(A4)	A60
VIDF	A	P90(A18)	A60
VIDH	A	P90(19)	A60

**A90 ANALOG DISPLAY DRIVER**  
03561-66590  
REV A

A90 Assembly

	+12 <sub>V1</sub>	-12 <sub>V1</sub>	+5V	GND
U1	4	11	14	7
U501				
U600				



NOTE:  
SEE THE A90, A99 TROUBLESHOOTING  
PROCEDURES FOR INSTRUCTIONS ON  
SELECTING CAPACITORS C5, C6, C7, AND C8.  
\* CAPACITORS C5, C6, C7 AND C8  
ARE RESELECTED WHENEVER T100  
IS REPLACED.

**7-39 A99 MOTHERBOARD ASSEMBLY**

**7-40 Motherboard Circuit Description**

The primary function of the motherboard assembly is to interconnect the signals of all -hp-3561A circuit assemblies. In addition to signal interconnect, the Motherboard Assembly contains part of the power supply circuits and part of the analog display driver circuits. Troubleshooting information for the power supply circuits is included with the A70, A71, and A72 Assemblies troubleshooting information. Troubleshooting information for the analog display circuits is included with the A90 Assembly troubleshooting information. Table 7-64 lists all inter-assembly signal connections.

**Table 7-64 Signal Interconnect**

Connector Number →	<b>J15</b>	J62
Pin Number →→	<b>B13</b>	A13
	↑	↑
	Signal	Signal
	Origin	Destination
	(Shown in bold)	



Control and I/O Signals

Signal Name	Assemblies														
	A10	A15	A20	A30	A40	A50	A60	A65 A66	A70	A71	A72	A81	A82	A90	A99
A/D DATA		<b>J15</b> <b>B13</b>	J22 A2												
ATN I/O BEEP						J52 A18							J82 A14		
$\overline{\text{BUBI}}$					J41 A6		<b>J62</b> <b>B8</b>				J72 B16				
$\overline{\text{BUBS}}$					<b>J41</b> <b>A10</b> <b>J41</b> <b>B10</b>			<b>J65</b> <b>A15</b> J65 B16 J65 B18							
$\overline{\text{CMOSS}}$															
COMP	<b>J10</b> <b>B25</b>	J15 B1													
CONVERT		J15 B16	<b>J22</b> <b>B2</b>												
COSINE			J21 A19			<b>J51</b> <b>B8</b>									
DAV I/O $\overline{\text{DATAREQ}}$						J52 B16							J82 A9		
$\overline{\text{DMAI}}$		J15 B14	<b>J22</b> <b>B3</b> <b>J21</b> <b>B16</b>		J41 A7										
$\overline{\text{DSPH}}$					J41 B5		<b>J61</b> A7								
$\overline{\text{DSPS}}$					<b>J41</b> A9		J61 A8								
$\overline{\text{DF1BG}}$			J22 A11	<b>J32</b> <b>B12</b>											
$\overline{\text{DF2BG}}$			J22 A10	<b>J32</b> <b>B13</b>											
$\overline{\text{DF3BG}}$			J22 A9	<b>J32</b> <b>B14</b>											
$\overline{\text{DF1BR}}$			<b>J22</b> <b>B11</b>	J32 A12											
$\overline{\text{DF2BR}}$			<b>J22</b> <b>B10</b>	J32 A13											
$\overline{\text{DF3BR}}$			<b>J22</b> <b>B9</b>	J32 A14											
ESR*4			<b>J21</b> <b>A23</b>			J51 B3									
EOI I/O						J52 B15							J82 A8		

Control and I/O Signals

Signal Name	Assemblies														
	A10	A15	A20	A30	A40	A50	A60	A65 A66	A70	A71	A72	A81	A82	A90	A99
EXT SAMP			J22 A7										J82 B18		
EXT TRIG						J52 A8							J82 A18		
FECAL	J10 A15		J21 B12												
$\overline{\text{FECLKI}}$	J10 A24	J15 A2													
FECLK	J10 A16		J21 B11												
FEDATA	J10 B16		J21 A11												
FEDATAIC	J10 A25	J15 A1													
$\overline{\text{FEISO}}$			J21 B14												
FELATCHI	J10 A23	J15 A3													
FELATCH	J10 B15		J21 A12												
FETRIG		J15 A13	J22 B5												
$\overline{\text{FFTI}}$				J31 B4	J41 A8										
$\overline{\text{FPS}}$					J41 B8							J81 B14			
FSYNC							J61 B4								J90 B6
$\overline{\text{HPCI}}$					J41 B7	J51 A7									
$\overline{\text{HPDI}}$					J41 B6	J51 A6									
$\overline{\text{HPIBS}}$					J41 B11	J51 A11									
IFC I/O ISA						J52 A16			J70 A10 B10	J71 A16			J82 A12		
ISB									J70 A9 B9	J71 B16					
ISM	J10 B23	J15 A6													
$\overline{\text{LOS}}$					J41 A11	J51 A10									
$\overline{\text{LOW}+5}$					J42 B13				J70 B13						
LSYNC							J62 B9			J71 A10					
NDAC I/O						J52 B18							J82 A11		

Control and I/O Signals

Signal Name	Assemblies															
	A10	A15	A20	A30	A40	A50	A60	A65 A66	A70	A71	A72	A81	A82	A90	A99	
NRFD I/O NOISE						J52 B17 J52 B21							J82 A11 J6		J300	
$\overline{\text{PBG}}$				J32 B16	J42 B16											
$\overline{\text{PBLDS}}$				J31 A6	J41 A12											
$\overline{\text{PBR}}$				J32 A16	J42 A16											
$\overline{\text{PBR/W}}$				J31 B7	J41 B13	J51 A13	J61 A13	J65 B15				J81 B13				
$\overline{\text{PBUDS}}$				J31 B6	J41 A13	J51 B13										
PDRIVE														J90 A9 B9	A99 T1	
$\overline{\text{PRAMRE}}$				J31 A7	J41 A4											
$\overline{\text{PRIOS}}$				J32 B17	J42 B17											
PRN SYNC						J52 A21							J82 B19			
PSENSE														J90 A11 B11	A99 T100	
$\overline{\text{RBR/W}}$			J21 A10	J31 B16												
$\overline{\text{PWR FAIL}}$					J41 A4					J71 A11						
REN I/O						J52 A15							J82 B8			
$\overline{\text{RESET}}$			J21 A21	J31 B3	J41 B3	J51 A3	J61 A3	J65 B17				J81 B17				
$\overline{\text{RIOS}}$			J21 B10	J31 A16												
$\overline{\text{SINT}}$					J41 B12	J51 A12										
-SINE			J21 B19			J51 A8										
SRQ I/O						J52 A17							J82 A13			
SSTAT		J15 A14	J22 B4													
SSYNC							J61 B5							J90 B4		
SYNC2			J21 B18			J51 A5										
TRIG LVL	J10 B24	J15 B2														
VIDF							J61 B3							J90 A18		

Control and I/O Signals

Signal Name	Assemblies															
	A10	A15	A20	A30	A40	A50	A60	A65 A66	A70	A71	A72	A81	A82	A90	A99	
VIDH							<b>J61 B2</b>							J90 A19		
ZPHTRIG			<b>J21 A17</b>			J51 A9										
1/3TRIG			J22 B7			<b>J52 A6</b>										
Data and Address Bus Signals																
DIO1 I/O						J52 B11							J82 A4			
DIO2 I/O						J52 B12							J82 A5			
DIO3 I/O						J52 B13							J82 A6			
DIO4 I/O						J52 B14							J82 A7			
DIO5 I/O						J52 A11							J82 B4			
DIO6 I/O						J52 A12							J82 B5			
DIO7 I/O						J52 A13							J82 B6			
DIO8 I/O						J52 A14							J82 B7			
PAB0					<b>J41 B16</b>	J51 B16	J61 B16	J65 A12					J81 B11			
PAB1					<b>J41 A16</b>	J51 A16	J61 A16	J65 B12					J81 A11			
PAB2					<b>J41 B15</b>	J51 B15	J61 B15	J65 A13								
PAB3					<b>J41 A15</b>		J61 A15	J65 B13								
PAB4					<b>J41 B14</b>			J65 A14								
PAB5					<b>J41 A14</b>			J65 B14								
PDB0 I/O				J31 B15	J41 B24	J51 B24	J61 B24	J65 A4					J81 B6			
PDB1 I/O				J31 A15	J41 A24	J51 A24	J61 A24	J65 B4					J81 A6			
PDB2 I/O				J31 B14	J41 B23	J51 B23	J61 B23	J65 A5					J81 B7			
PDB3 I/O				J31 A14	J41 A23	J51 A23	J61 A23	J65 B5					J81 A7			
PDB4 I/O				J31 B13	J41 B22	J51 B22	J61 B22	J65 A6					J81 B8			
PDB5 I/O				J31 A13	J41 A22	J51 A22	J61 A22	J65 B6					J81 A8			
PDB6 I/O				J31 B12	J41 B21	J51 B21	J61 B21	J65 A7					J81 B9			
PDB7 I/O				J31 A12	J41 A21	J51 A21	J61 A21	J65 B7					J81 A9			
PDB8 I/O				J31 B11	J41 B20	J51 B20	J61 B20	J65 A8								

Data and Address Bus Signals

Signal Name	Assemblies															
	A10	A15	A20	A30	A40	A50	A60	A65 A66	A70	A71	A72	A81	A82	A90	A99	
PDB9 I/O				J31 A11	J41 A20	J51 A20	J61 A20									
PDBA I/O				J31 B10	J41 B19	J51 B19	J61 B19									
PDBB I/O				J31 A10	J41 A19	J51 A19	J61 A19									
PDBC I/O				J31 B9	J41 B18	J51 B18	J61 B18									
PDBD I/O				J31 A9	J41 A18	J51 A18	J61 A18									
PDBE I/O				J31 B8	J41 B17	J51 B17	J61 B17									
PDBF I/O				J31 A8	J41 A17	J51 A17	J61 A17	J65 B11								
RAB0 I/O			J21 A2	J31 B24	J42 B11											
RAB1 I/O			J21 B2	J31 A24	J42 A11											
RAB2 I/O			J21 A3	J31 B23	J42 B10											
RAB3 I/O			J21 B3	J31 A23	J42 A10											
RAB4 I/O			J21 A4	J31 B22	J42 B9											
RAB5 I/O			J21 B4	J31 A22	J42 A9											
RAB6 I/O			J21 A5	J31 B21	J42 B8											
RAB7 I/O			J21 B5	J31 A21	J42 A8											
RAB8 I/O			J21 A6	J31 B20	J42 B7											
RAB9 I/O			J21 B6	J31 A20	J42 A7											
RABA I/O			J21 A7	J31 B19	J42 B6											
RABB I/O			J21 B7	J31 A19	J42 A6											
RABC I/O			J21 A8	J31 B18	J42 B5											
RABD I/O			J21 B8	J31 A18	J42 A5											
RABE I/O			J21 A9	J31 B17	J42 B4											
RABF I/O			J21 B9	J31 A17	J42 A4											
RDB0 I/O			J22 A12	J32 B11												
RDB1 I/O			J22 B12	J32 A11												

Data and Address Bus Signals

Signal Name	Assemblies															
	A10	A15	A20	A30	A40	A50	A60	A65 A66	A70	A71	A72	A81	A82	A90	A99	
RDB2 I/O			J22 A13	J32 B10												
RDB3 I/O			J22 B13	J32 A10												
RDB4 I/O			J22 A14	J32 B9												
RDB5 I/O			J22 B14	J32 A9												
RDB6 I/O			J22 A15	J32 B8												
RDB7 I/O			J22 B15	J32 A8												
RDB8 I/O			J22 A16	J32 B7												
RDB9 I/O			J22 B16	J32 A7												
RDBA I/O			J22 A17	J32 B6												
RDBB I/O			J22 B17	J32 A6												
RDBC I/O			J22 A18	J32 B5												
RDBD I/O			J22 B18	J32 A5												
RDBE I/O			J22 A19	J32 B4												
RDBF I/O			J22 B19	J32 A4												
<b>Clocks</b>																
100 kHz				J31 B2	<b>J41</b> <b>A3</b>											
256 kHz			<b>J21</b> <b>B23</b>						J70 B8							
4 MHz					<b>J41</b> <b>B2</b>	J51 A2		J65 A17								
10.24 MHz		J15 A15	<b>J21</b> <b>A24</b>			J51 B2										
20.48 MHz		J15 B15	J21 B24	J31 A2	<b>J41</b> <b>A2</b>											
<b>Common Ground Power Supplies</b>																
+5V	J10 A13 B13	J15 A8 B8	J22 A21 B22 B22	J32 A1 B1 B2	J42 A1 B1 B2	J52 A1 B1	J62 A1 B1 B2	J65 A21 A22 B21 B22	J70 A11 B11	<b>J71</b> <b>A13</b> <b>A14</b> <b>A15</b> <b>B14</b> <b>B15</b>		J81 A19 A20 B19 B20	J82 A2 B2	J90 A4 B7 B19		
+8V			J22 B21													<b>A99</b> <b>U203</b>

**Common Ground Power Supplies**

Signal Name	Assemblies															
	A10	A15	A20	A30	A40	A50	A60	A65 A66	A70	A71	A72	A81	A82	A90	A99	
+12V <sub>A</sub>									J70 A7					J90 A2 A7 A21 B2 B21	<b>A99 U200</b>	
+12V <sub>B</sub>		J15 A9 B9	J22 A20		J42 B3	J52 B3	J62 B3	J65 A20	J70 A8							<b>A99 U201</b>
-12V		J15 A10 B10	J22 B20		A3	J52			J70 B6				J82 B20	J90 A3 A20 B3 B20	<b>A99 U202</b>	
+5V <sub>ref</sub>									<b>J70 A13</b>	J71 A9						
+12VBIAS									J70 A16 A17 B16 B17	<b>J71 A5 A6</b>						
-12VBIAS									J70 A14 A15 B14 B15	<b>J71 A7 A8</b>						
+450 Vpeak														J90 B15	<b>A99 T100</b>	
-150 Vpeak														J90 A15	<b>A99 T100</b>	
<b>Isolated Ground Power Supplies</b>																
+5V <sub>A1</sub>		J15 A21 B21							J70 B3							<b>A99 U204</b>
+5V <sub>B1</sub>	J10 A21 B21								J70 B2							<b>A99 U205</b>
+15V <sub>1</sub>	J10 A18 B18	J15 A18 B18							J70 B1							<b>A99 U301</b>
+24V <sub>1</sub>	J10 A11 B11								J70 A1							<b>A99 U302</b>
-15V <sub>1</sub>	J10 A17 B17	J15 A19 B19							J70 A2							<b>A99 U300</b>

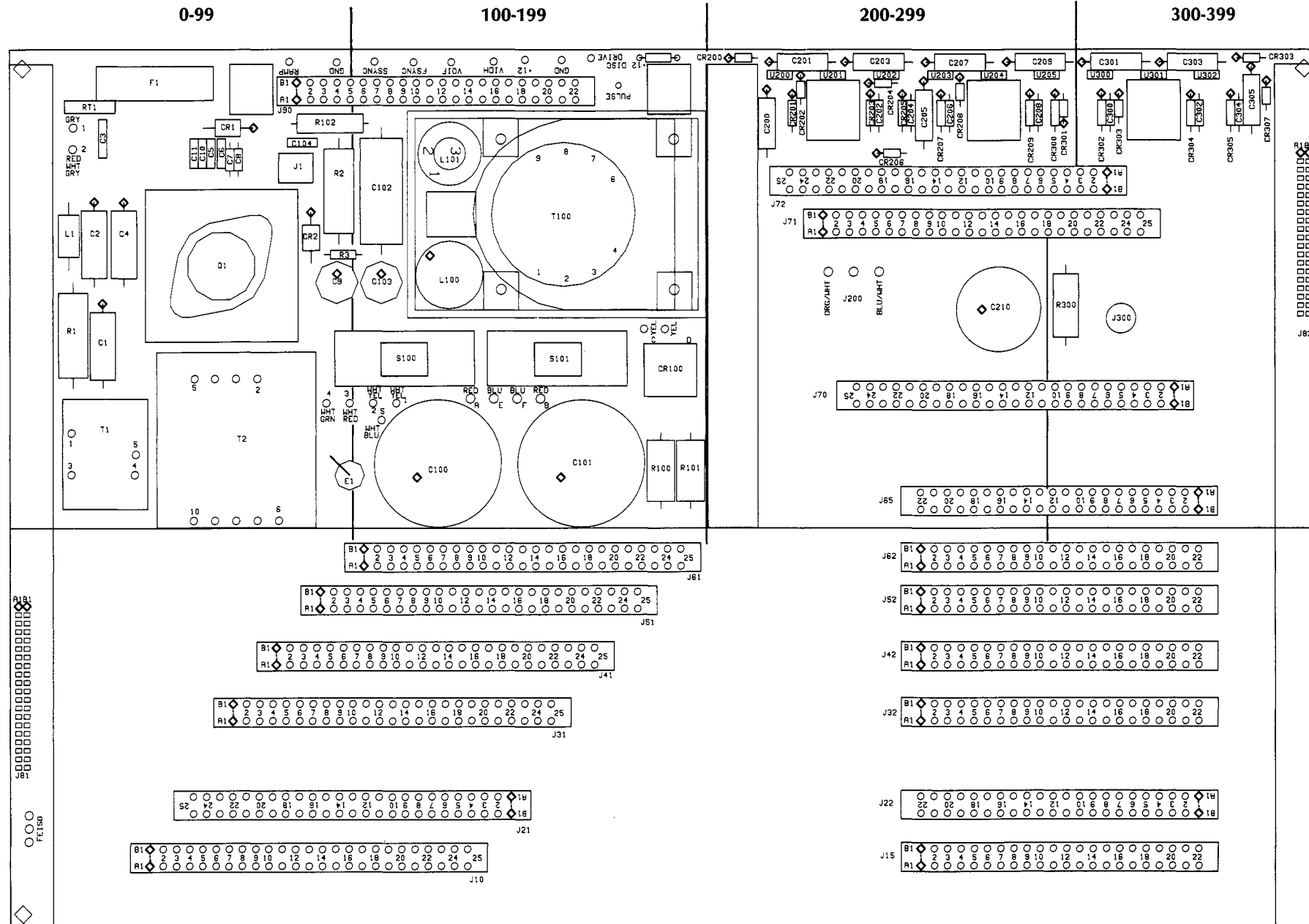
Unregulated Power Supplies

Signal Name	Assemblies															
	A10	A15	A20	A30	A40	A50	A60	A65 A66	A70	A71	A72	A81	A82	A90	A99	
+8V <sub>U</sub> (+12V)											J72 A18 A19				A99 U203	
+12V <sub>U</sub> (+15V)											J72 A22 A23 A24 A25			J90 B18	A99 U200 U201	
-12V <sub>U</sub> (-15V)											J72 A16 A17 A20 A21		J82 A1 B1		A99 U202	
+5V <sub>UI</sub> (+8VI)									J70 A3		J72 A7 A8 A9				A99 U204 U205	
+15V <sub>UI</sub> (+19VI)											J72 A3 A4				A99 U301	
+24V <sub>UI</sub> (+27VI)											J72 A1 A2				A99 U302	
-15V <sub>UI</sub> (-19VI)											J72 A5 A6				A99 U300	
Raw Power Supplies (unfiltered)																
+8V <sub>R</sub>											J71 B7 B8	J72 B18 B19				
+12V <sub>R</sub>											J71 B1 B2 B3 B4	J72 B22 B23 B24 B25				
-12V <sub>R</sub>											J71 B5 B6	J72 B20 B21				
+5V <sub>IR</sub>											J71 A22 B22	J72 B7 B8 B9				
+15V <sub>IR</sub>											J71 A24 B24	J72 B3 B4				
+24V <sub>IR</sub>											J71 A25 B25	J72 B1 B2				
-15V <sub>IR</sub>											J71 A23 B23	J72 B5 B6				



Line power supplies

Signal Name	Assemblies															
	A65															
	A10	A15	A20	A30	A40	A50	A60	A66	A70	A71	A72	A81	A82	A90	A99	
BIAS AC1										J71 A1 A2					A99 T2	
BIAS AC2										J71 A3 A4					A99 T2	
+170 Vdc									J700 1						J200 1 2	
-170 Vdc									J700 3						J200 3 4	



## APPENDIX A QUICK REFERENCE

This quick reference contains abbreviated operating information for the -hp-3561A. Included in this section is a brief description of the -hp-3561A front and rear panels, and a map illustrating the -hp-3561A menus.

### MENU DEFINED KEYS

The menu defined keys are defined by the display menu entries. Menus are selected and displayed by pressing a labeled front panel key.

### MEASUREMENT KEY GROUP

The measurement group indicators illuminate when a measurement is in progress, or measurement options are selected or enabled. The measurement group keys control the measurement and select menus for altering measurement parameters and options.

**EXT SAMP** indicator illuminates when the external sampling mode is enabled.

**AVG** key indicator illuminates when an averaging process is selected.

**TIME BUFFER** key indicator illuminates when the time capture mode is selected.

**MEAS** indicator illuminates when a measurement is in progress.

**MODE** key displays a menu for selecting the instrument measurement mode (narrow band, third octave, full octave, time capture, external sample, or test modes).

**AVG** key displays a menu for selecting the type of averaging process applied to the measurement.

**TIME BUFFER** key displays a menu for initiating a time capture operation and defining the time capture mode parameters.

**START** key clears the time record and accumulated average results, and initiates a measurement.

**FREQ** key displays a menu for defining the measurement frequency parameters.

**WINDOW** key displays a menu for selecting the window applied to the input signal.

**SOURCE** key displays a menu for enabling the -hp-3561A noise source and selecting the noise type.

**PAUSE/CONT** key suspends an in progress measurement or continues a suspended measurement.

### TRIGGER KEY GROUP

The trigger group keys control the trigger function. The trigger indicators illuminate to indicate the trigger status.

**TRIG SEL** key indicator illuminates when the -hp-3561A is triggered.

**TRIG SEL** key displays a menu for selecting and defining the trigger used for starting a measurement.

**ARM** key indicator illuminates when the -hp-3561A is armed and waiting for a valid trigger.

**ARM** key resets the trigger circuits when the manual arm trigger mode is selected.

### HP-IB KEY GROUP

HP-IB group keys control the HP-IB and plotting functions. HP-IB indicators illuminate to indicate the HP-IB status.

**RMT** indicator illuminates when the -hp-3561A is operating under HP-IB control. In the remote mode, (and the **LCL** key is not locked out by the controller), only the **LCL** key is recognized by the -hp-3561A.

**SRQ** indicator illuminates when the -hp-3561A generates an HP-IB service request.

**LTN** indicator illuminates when the -hp-3561A is addressed to listen over the HP-IB.

**TLK** indicator illuminates when the -hp-3561A is addressed to talk over the HP-IB.

**LCL** key displays a menu for setting the HP-IB address, enabling the talk only mode, and enabling the HP-IB power on service request.

**PLOT** key displays a menu for selecting and defining plotter options.

### LINE KEY

**LINE** key applies power to the -hp-3561A circuits.

### DISPLAY KEY GROUP

The display group keys affect the display format.

**NEXT TRACE** key selects the active trace on the display. For a single trace format, **NEXT TRACE** toggles the display between the two available traces. The active trace is the trace displayed. For an upper/lower trace format, the active trace is identified by an intensified label over the trace graticule. For a front/back trace format or map format, the active trace is intensified.

**DEFINE TRACE** key displays a menu for selecting the magnitude, phase, time, or math trace functions.

**VERT SCALE** key displays a menu for scaling the vertical display axis.

**STORE/RECALL** key displays a menu for storing traces in memory, recalling traces from memory, and entering trace labels.

**UNITS** key displays a menu for selecting and defining the vertical and horizontal axis units of the display.

**FORMAT** key displays a menu for selecting a single trace, upper/lower trace, front/back trace, or map display format.

### MARKER GROUP KEYS

The marker group keys affect the operation of the marker. The **◀**, **FAST**, and **▶** keys position the marker on the active trace. **FAST**, when used with the arrow keys, moves the marker at a faster rate.

**MKR** key displays a menu for selecting absolute marker functions.

**SPCL MKR** key displays a menu for selecting band marking, harmonic marker, and sideband marker measurements.

**REL MKR** key displays a menu for enabling the relative marker function and defining the reference values for the relative measurements.

### INSTRUMENT STATE KEY GROUP

The instrument state group keys affect the instrument setup configuration.

**SAVE** key displays a menu for storing the current instrument state in nonvolatile memory.

**RECALL** key displays a menu for recalling an instrument state from nonvolatile memory.

**VIEW ON/OFF** key toggles the display between a graphic trace display and a tabular text display of the instrument state.

**PRESET** key initializes the -hp-3561A to the most commonly required setup.

### INPUT KEY GROUP

The input group keys control the -hp-3561A input circuits. The input group indicators provide an indication of the input circuit status.

**OVER** indicator illuminates when the input signal amplitude exceeds the maximum range of the signal processing circuits.

**HALF** indicator illuminates when the input signal level is greater than one-half the maximum input range value. An optimum input level illuminates the **HALF** indicator without illuminating the **OVER** indicator.

**AUTO** indicator illuminates when the -hp-3561A auto-ranging circuits are enabled.

**ICP CURRENT** indicator illuminates when the -hp-3561A ICP current source is enabled.

**A WT FILTER** indicator illuminates when an internal A-weighting filter is in the -hp-3561A input signal path.

**AC COUPLE** indicator illuminates when ac coupling is selected.

**RANGE** key displays a menu for setting the input range or selecting auto-range.

**INPUT** key displays a menu for selecting the -hp-3561A input circuits (ac/dc coupling, A-weighting filter, or ICP current source) or calibration circuits.

**FLOAT-CHASSIS** switch connects the input circuit ground reference to chassis ground or isolates (floats) it from chassis ground.

### WARNING

*Do not isolate the -hp-3561A from earth ground by interrupting the protective earth conductor inside or outside the -hp-3561A. Interruption of the protective earth conductor can subject the operator to lethal voltages.*

**INPUT** connector provides a high impedance input (1 MΩ).

### REAR PANEL CONNECTORS

**SOURCE OUTPUT** connector is the output for the -hp-3561A pseudo-random noise source or impulse generator. This output is enabled through the **SOURCE** key menu.

A positive **SOURCE SYNC** output marks a time record that coincides with an impulse or pseudo-random noise output. The output occurs at the start of the time record. If the trigger is derived from the internal noise source or impulse generator, the output is synchronized to the source trigger signal. The **SOURCE SYNC** output is a TTL level pulse.

The -hp-3561A sampling frequency is controlled through the **EXT SAMPLE** connector when the external sampling mode is enabled through the **MODE** key. The **EXT SAMPLE** input is TTL compatible.

External trigger sources connect to the -hp-3561A through the **EXT TRIGGER** input connector. The -hp-3561A trigger circuits sense this connector when **EXTERNAL TRIGGER** is selected through the **TRIG SEL** key menu. The trigger input is TTL compatible.

External HP-IB devices communicate with the -hp-3561A through the rear panel HP-IB connector. The -hp-3561A controls a printer or plotter through this connector.

### CROSS REFERENCE TO CHAPTER II OPERATOR'S REFERENCE

KEY/KEY GROUP	PAGE
AC COUPLE INDICATOR	95
ARM KEY/INDICATOR	73
AUTO INDICATOR	95
AVG KEY/INDICATOR	63
A WT FILTER INDICATOR	95
BACK SPACE KEY	74
DEFINE TRACE KEY	78
<b>DISPLAY KEY GROUP</b>	78
DOWN ARROW KEY	74
EXT SAMPLE CONNECTOR	97
EXT SAMPLE INDICATOR	60
EXT TRIG CONNECTOR	98
FAST KEY	88
FLOAT - GROUND SWITCH	97
FREQ KEY	69
FORMAT KEY	86
HALF INDICATOR	95
HP-IB CONNECTOR	97
<b>HP-IB KEY GROUP</b>	75
ICP CURRENT INDICATOR	95
INPUT CONNECTOR	97
INPUT KEY	96
<b>INPUT KEY GROUP</b>	95
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LEFT ARROW KEY	88
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MKR VALUE KEY	74
NEXT TRACE KEY	78
<b>NUMERIC ENTRY KEYS</b>	74
OVER INDICATOR	95
PAUSE/CONT KEY	71
PLOT KEY	76
PRESET KEY	93
RANGE KEY	95
<b>REAR PANEL CONNECTORS</b>	97
RECALL KEY	92
REL MKR KEY	90
RETURN KEY	60
RIGHT ARROW KEY	88
RMT INDICATOR	75
SAVE KEY	91
SOFTKEYS	59
SOURCE KEY	71
SOURCE OUT CONNECTOR	98
SOURCE SYNC CONNECTOR	98
SPCL MKR KEY	89
SRQ INDICATOR	75
START KEY	69
STORE/RECALL KEY	84
TALK INDICATOR	75
TIME BUFFER KEY/INDICATOR	66
<b>TRIG KEY GROUP</b>	72
TRIG SEL KEY/INDICATOR	72
UNITS KEY	85
UP ARROW KEY	74
VERT SCALE KEY	83
VIEW ON/OFF KEY	93
WINDOW KEY	70

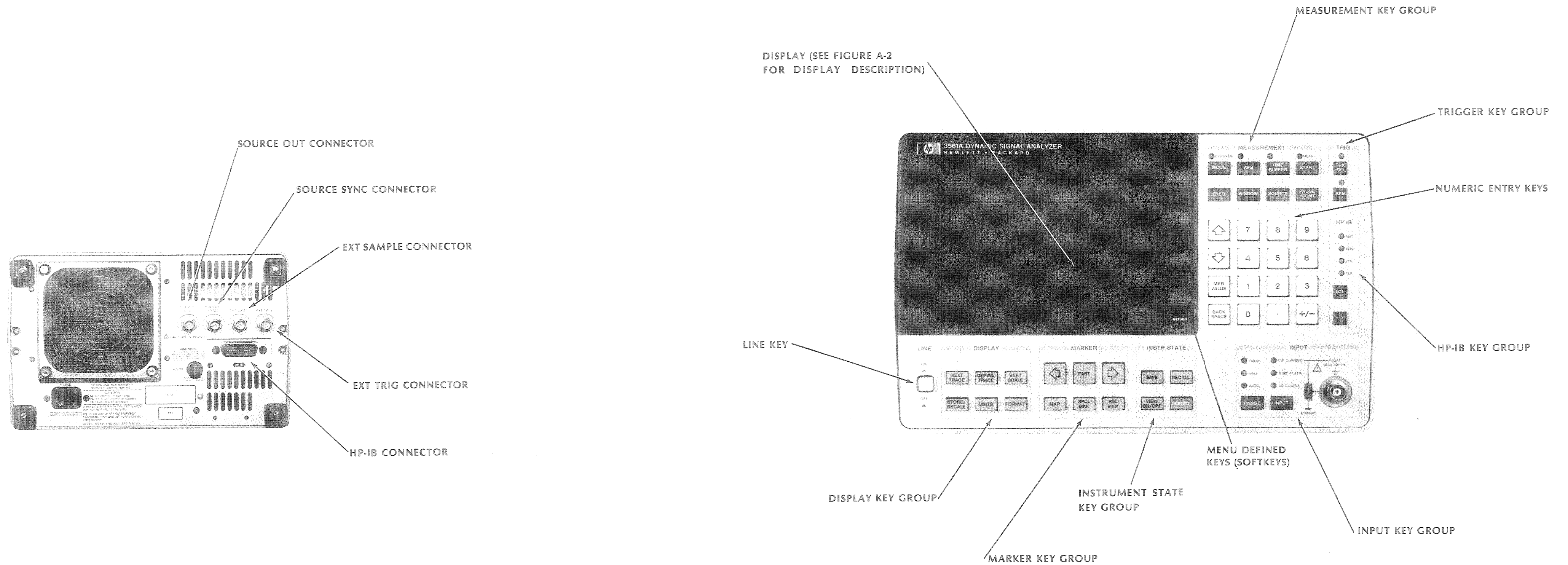


Figure A-1. -hp-3561A Front and Rear Panels. 1

**DISPLAY DESCRIPTION**

**ENTRY AREA** displays the alphanumeric characters used in defining a parameter. The current entry for a key requiring a numeric or character input is displayed here when the key is selected.

**INPUT RANGE** area displays the full scale input range.

**STATUS AREA** displays the current status of the -hp-3561A.

**TRACE DESCRIPTION** indicates the trace function. An intensified trace description indicates the active trace.

**TRACE LABEL** displays the trace annotation entered through the **DEFINE** **TRACELBL** menu entry when the trace label display is enabled. If the trace label display is disabled, a detailed description of the trace function is displayed in this area.

**AVERAGE STATUS** area provides information regarding the averaging process applied to the measurement.

**OVERLOAD STATUS** area indicates overloads occurring during a measurement.

**Y-AXIS LABEL** displays the annotation for the graticule vertical axis.

**X-AXIS LABEL** displays the annotation for the graticule horizontal axis.

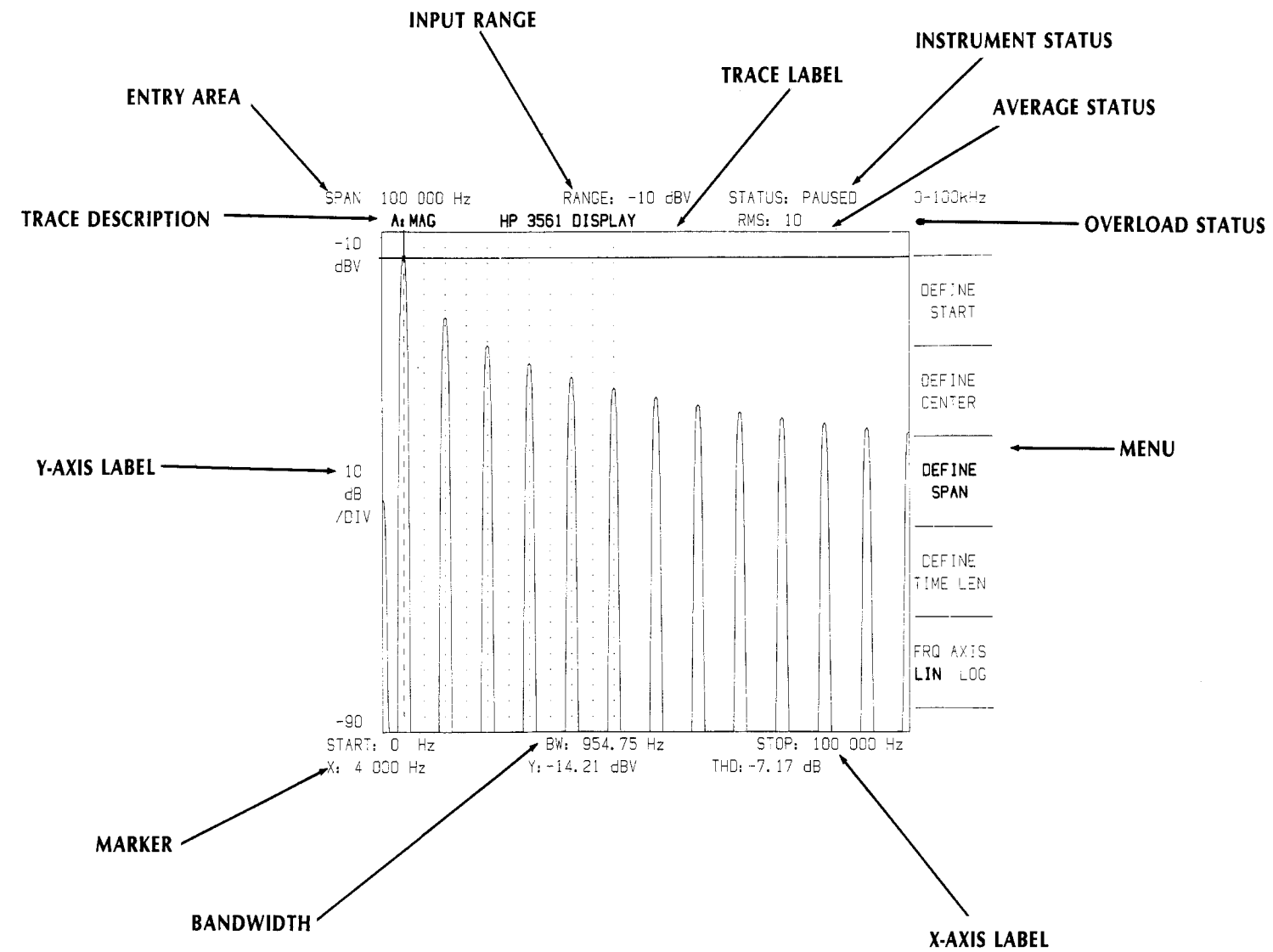
**BANDWIDTH** display area displays the measurement bandwidth.

**X MARKER** area displays the horizontal axis coordinate value of the marker.

**Y MARKER** area displays the vertical axis coordinate value of the marker.

**MENU** area displays the menu defining the unlabeled keys to the right of the menu.

**SINGLE TRACE AND MAP MODE DISPLAY FORMAT**



**DUAL TRACE DISPLAY FORMAT**

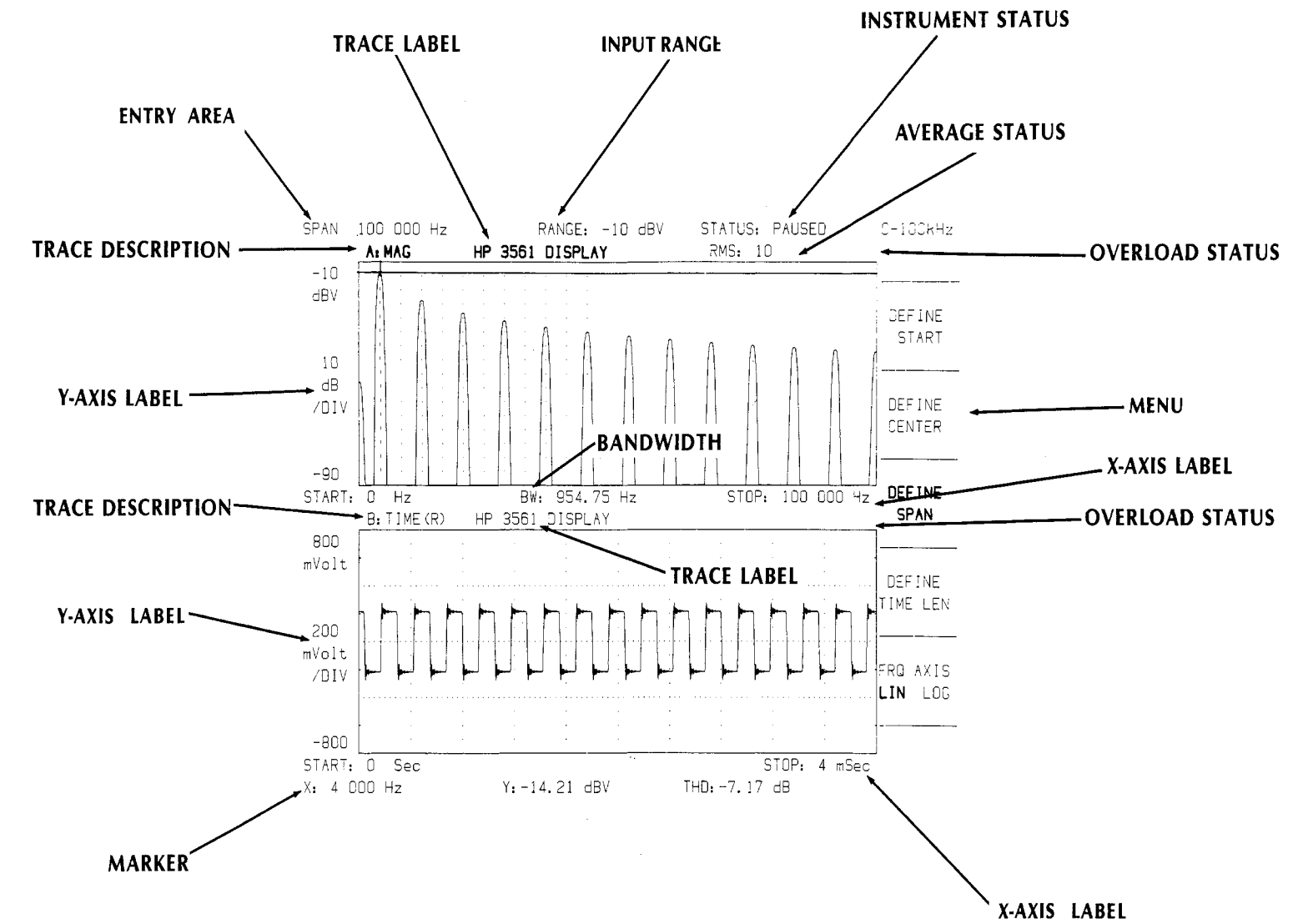
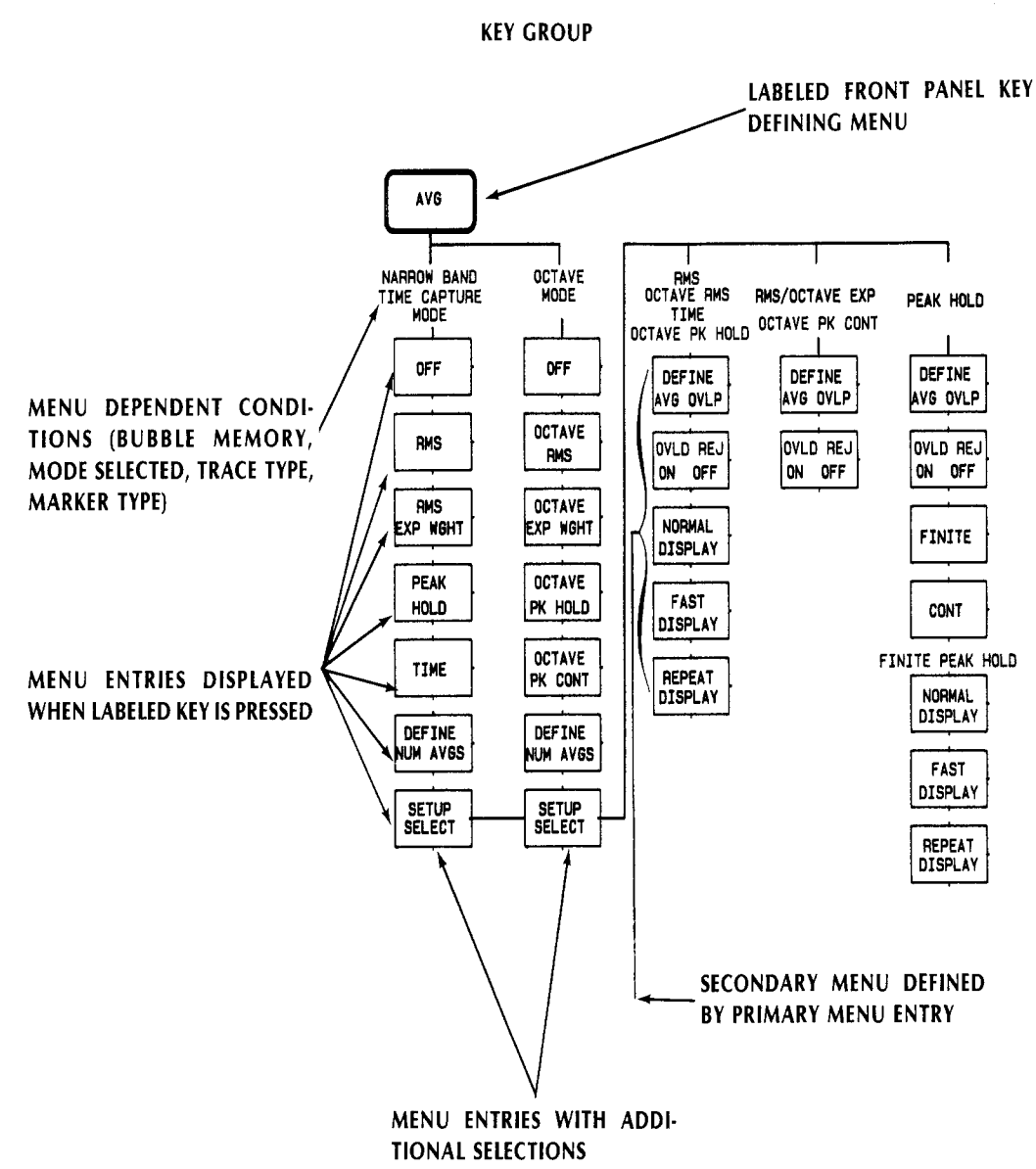
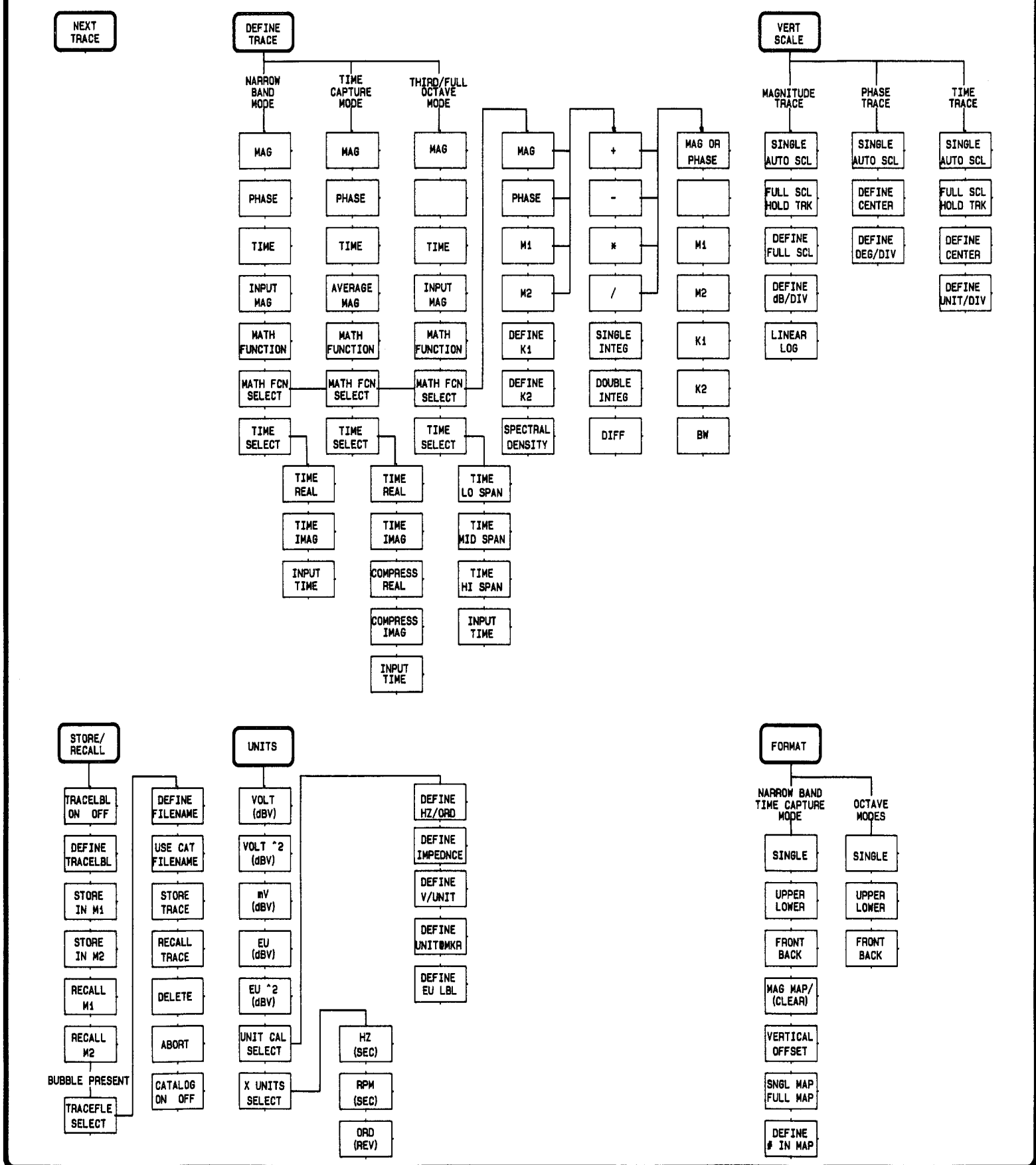


Figure A-2. Display Annotation II

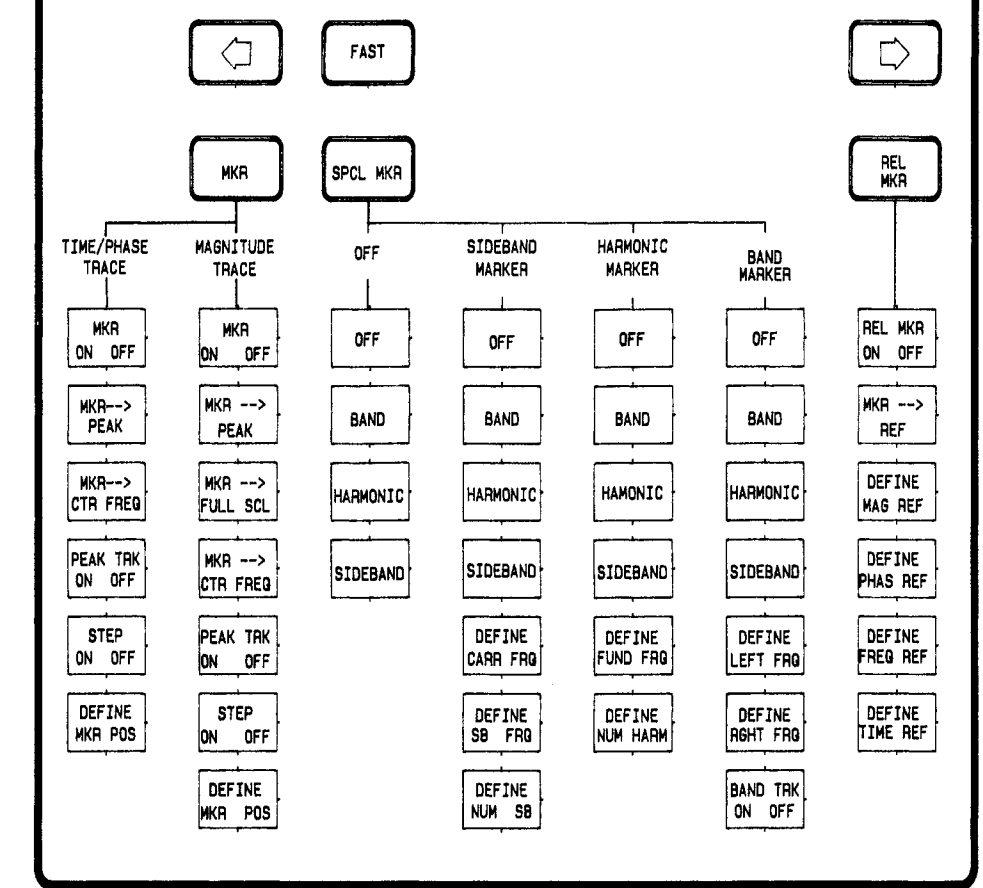
HOW TO INTERPRET THE KEY MAP



DISPLAY



MARKER



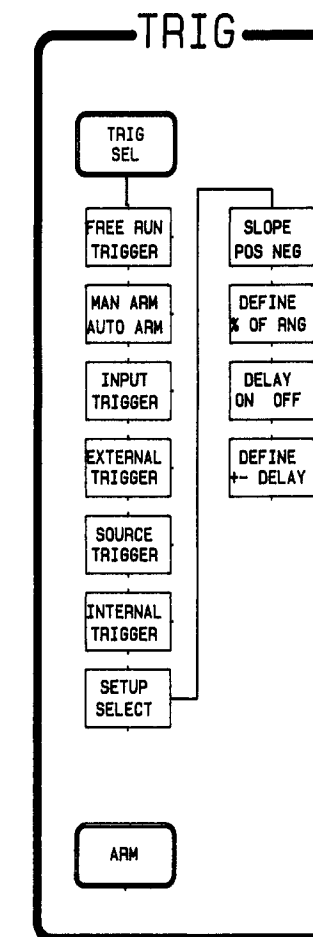
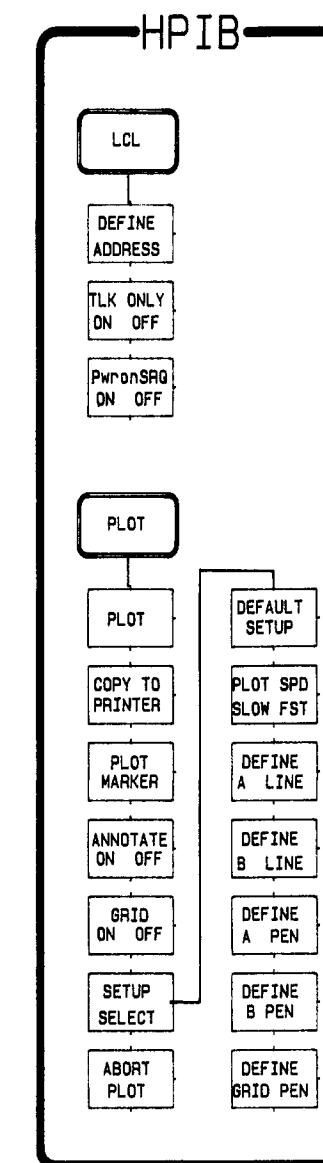
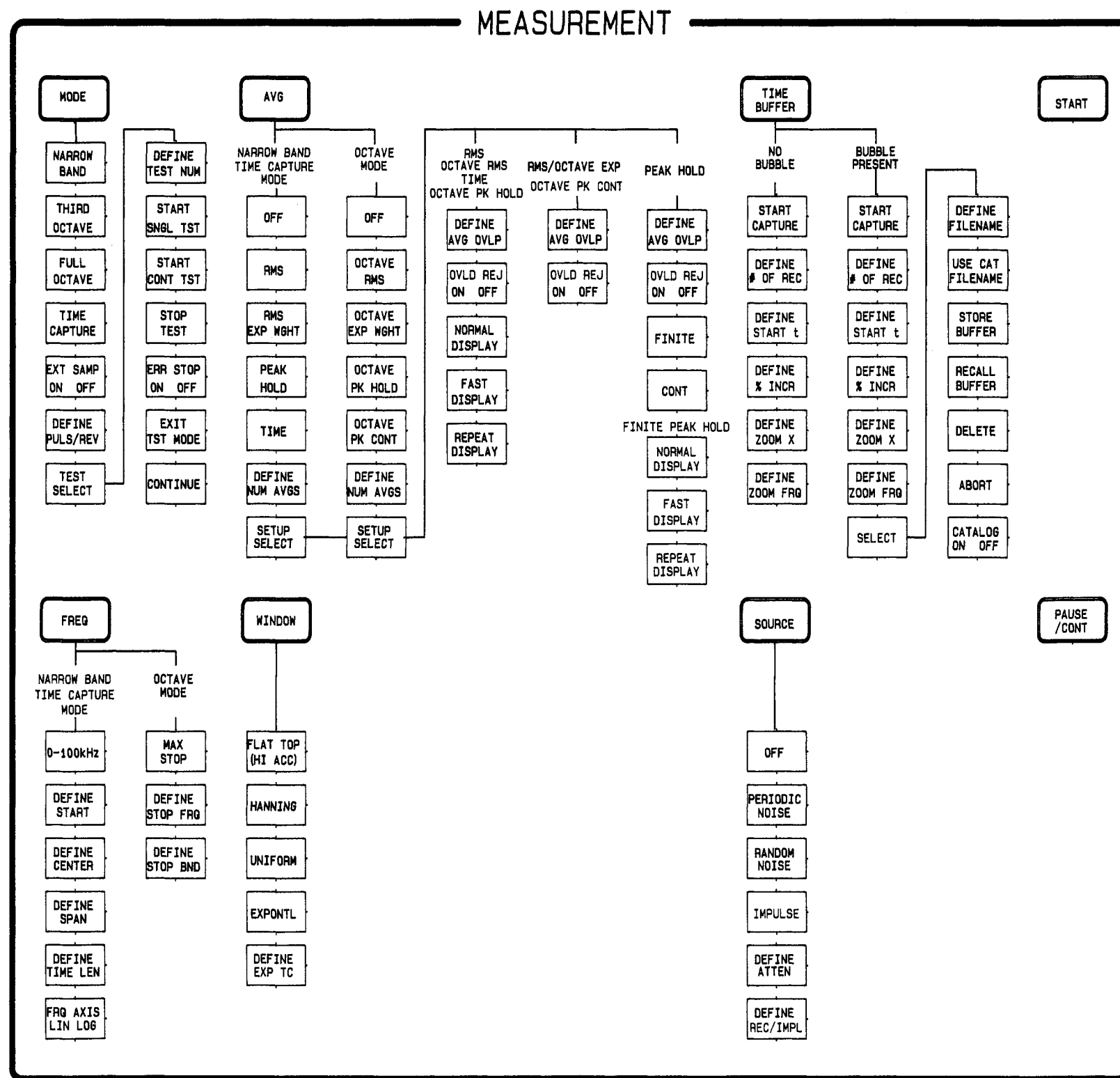
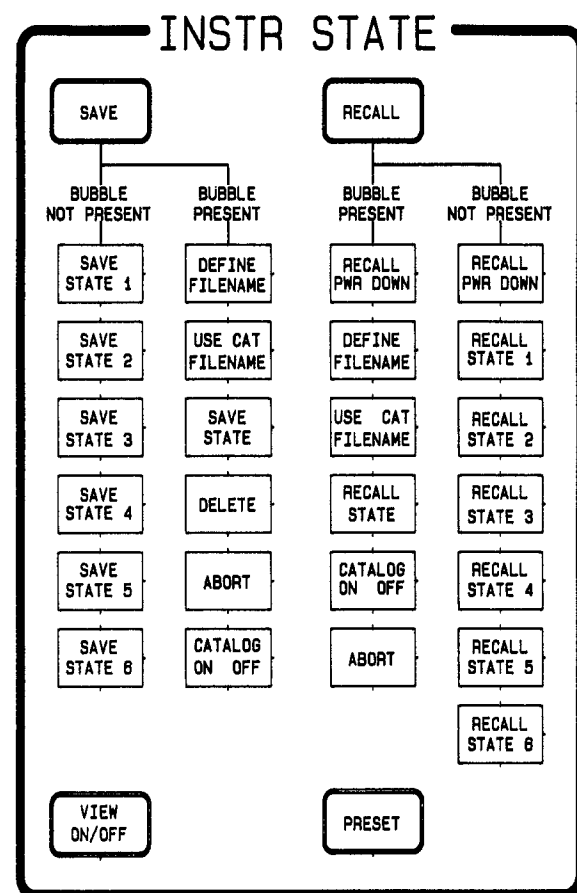
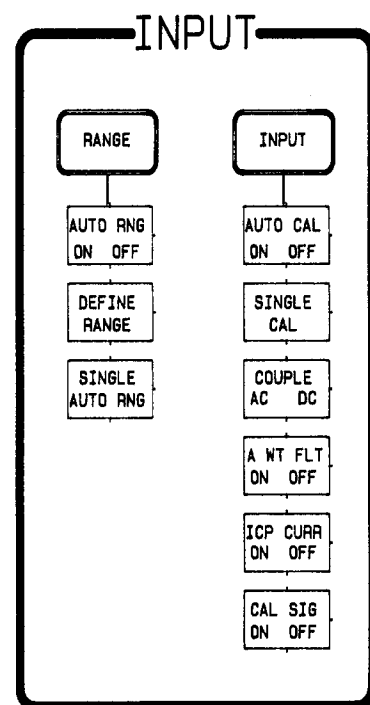


Figure A-3. -hp-3561A Menus Sheet 2



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